

Behavioral group meeting held on November 15, 2002

Present

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Issues

- Upcoming December review
- Boeing designs
- Plans for immediate future

Discussion result

List of things to be completed for the review:

Minimum

- Be able to simulate one complete design using BMAC compiler and compare the results against the benchmark

Maximum

Simulate three possible designs:

- Kishore's A/D converter design
- Boeing's auto-zero amplifier
- A/D converter block from Boeing's digital belt design

Using three different ways:

- In Cadence, with Verilog device models
- In Spice, with standard Spice models
- Using BMAC compiler/simulator

And the following models:

- BSIM3
- EKV

DAC paper:

In the view of little time left for the review and problems with BMAC compiler, leave paper writing for later (don't submit to DAC) and concentrate on getting results for the review.