High-Voltage Compliant, Electrode-Invariant Neural Stimulation Electronics
Compatible with Low-Voltage, Bulk-CMOS Integration

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Abstract

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This work explores the challenges of implementing practical, electrical neural stimulation interfaces using modern silicon CMOS technologies. To overcome said challenges, which stem from the discrepancy between the low-voltage limitations of modern CMOS devices and the large stimulation voltages often observed at response-evoking stimulus levels, a new stimulator front-end is proposed. The high-voltage compliant front-end can reliably drive biphasic, constant-current stimulus through a wide range of electrode impedances while being safely implemented in a low-voltage, bulk-CMOS technology. The topology of the front-end is based on a sink-regulated H-bridge. Stimulus current is supplied using specialized, fully-integrated dynamic voltage supplies (DVSs), which are controlled in closed-loop to have an output voltage approximately equal to the voltage of the electrode each supplies stimulus to. The entire stimulus

waveform is regulated by a single, low-voltage current-DAC, which can safely interface with the electrodes (which may be at high voltages) via specialized high-voltage adapter (HVA) circuits. To account for "capacitive-looking" electrodes and to provide unique, "electrode-invariant" performance, the front-end uses the balancing stimulus current to discharge the electrode-tissue-interface impedance (Z_E), and only after full Z_E discharge has been detected is a DVS used to supply the remaining balancing stimulus. In this thesis the described front-end topology and the enabling high-voltage operating circuits are presented and discussed in detail. Additionally, a stand-alone DVS circuit has been fabricated in 65nm bulk-CMOS, demonstrating the power-supplying and transient performance required by the proposed stimulator design. Another chip, featuring the entire integrated neural stimulator front-end, has also been designed in 65nm bulk-CMOS, with post-layout simulations showing ±11V compliance (approximately) across a 50µA to 2mA stimulus amplitude range. The efficacy of the proposed integrated electronics in potential neural stimulation applications is also explored using a board-level prototype and *in-vivo* evaluation.

TABLE OF CONTENTS

i

LIST OF FIGURES

LIST OF TABLES

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Chapter 1. INTRODUCTION

Electrical stimulation is commonly employed method of neural modulation, which, from a simplified perspective, relies on moving charge, in and out of neural tissue, to produce a desired level of neural activity (e.g. rate of action potential generation in targeted neurons). Apart from being a proven and indispensible research tool for probing the nervous system and investigating different neural circuits (in various animals, from vertebrates to invertebrates), electrical neural stimulation has found successful use in FDA-approved devices (retinal and cochlear implants, deep brain stimulation for Parkinson's disease and neuropsychiatric disorders, functional electrical stimulation of periphery nerves, etc.), and, in recent years, has gained traction as an important complement to neural-recording brain-computer interfaces (BCIs). In the latter, neural stimulation could be used as a direct means of closing the "BCI loop" to create "bidirectional" BCIs (i.e. BBCIs) and/or re-establishing brain control over paralyzed muscles [1]. Such closed-loop systems could lead to new and exciting neuroprostheses and rehabilitation methods [2] that, for practicality, would require robust, and likely implantable, neural interfaces that have neural stimulation capabilities.

Regardless of the implementation of a neural stimulation system, the requisite functionality, illustrated in Figure 1.1, remains for the most part fixed.
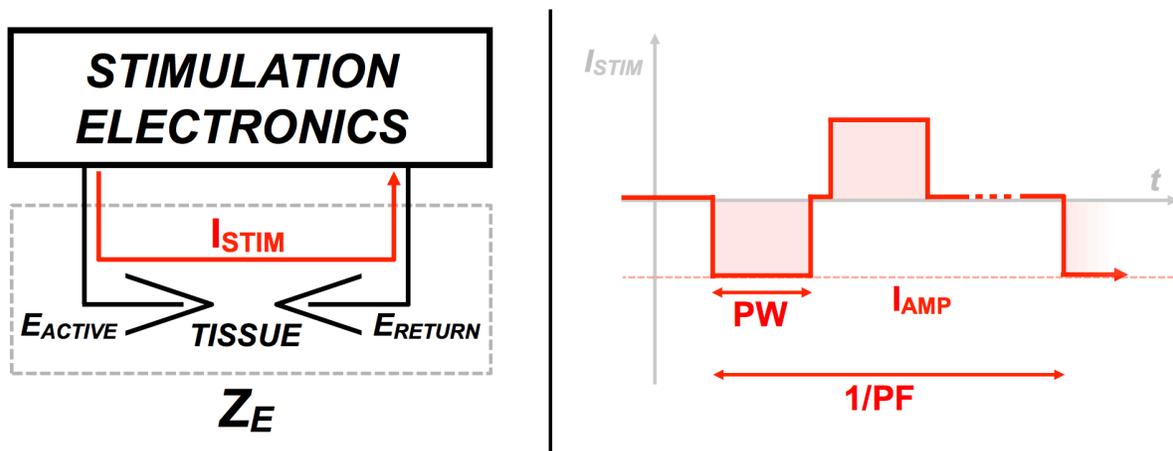
Figure 1.1. Requisite functionality of an electrical neural stimulation system.

As shown in Figure 1.1, the specialized front-end electronics of the stimulation system must be able to drive a charge-balanced current waveform between an "active" and "return" electrode, with the targeted neural tissue between said electrodes. The electrodes serve as the critical electronic-to-ionic current transducers, and together, the two electrodes and the tissue (through which the stimulus is driven) present the electrode-tissue-interface impedance, Z_E. Depending on the electrodes used, Z_E can be complex, as well as non-linear [3, 4].

However, in the literature pertaining to the design of electrode-interfacing electronics (e.g. neural recording and stimulation systems), Z_E is often modeled as a series R-C element, with R and C set to approximate the frequency response of a given electrode configuration [5-14]. However, a more realistic Z_E model includes a resistance in-parallel with the "C" of the said R-C model [3, 4, 15]. Accordingly, as shown in Figure 1.2, a $C_{DL}||R_{CT} + R_S$ electrode-tissue-interface impedance approximation can be used to more accurately model the frequency-dependent voltage observed across a given active-return electrode pair when applied current stimulus. In said approximation, C_{DL} models the "double-layer capacitance" transduction pathway; R_{CT}, the "charge-transfer" resistance, models the redox-driven transduction pathway; and R_S, the "spreading" or "solution" resistance, models the resistance to ionic current flow within the tissue [3, 4].
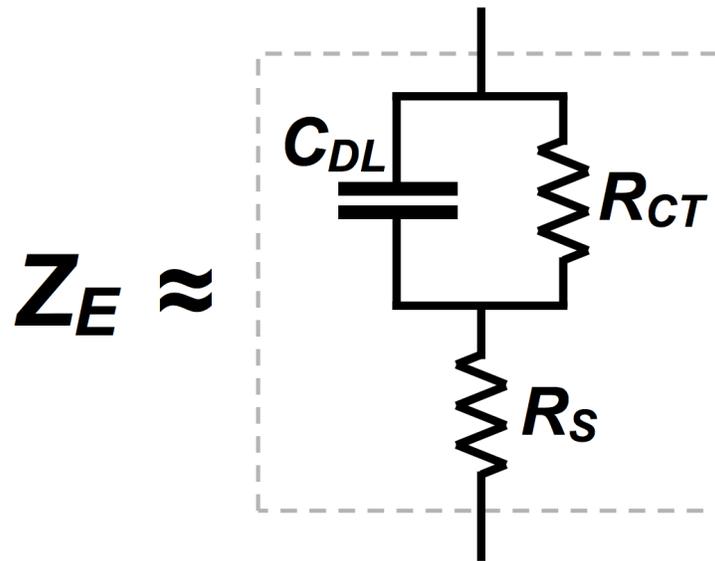
Figure 1.2. Electrode-tissue-interface impedance (Z_E) linear-circuit-element approximation.

A charge-balanced stimulus is not only recommend to protect tissue from damage, but also to limit electrode degradation over time [3]. The charge-balanced stimulus waveform itself may be current-regulated, voltage-regulated, or switched-capacitor regulated [6, 10], with said regulation schemes providing different tradeoffs in terms of the charge-balance precision, invariance to Z_E, power efficiency, circuit complexity, and overall safety [5, 6]. In terms of these potential stimulus regulation schemes, current-regulated stimulators are usually thought of as the "safest" in that the charge and current injected into the tissue, versus time, is completely regulated and known (i.e. not dependent on Z_E); therefore, such a stimulator can be easily programmed to deliver a charge-balanced current waveform (or close-to-such) which is well-defined from one Z_E impedance to the next.

Accordingly, many state-of-the-art stimulation systems today are designed to drive current-regulated "biphasic" stimulus pulses with constant-current amplitude (as shown in Figure 1.1) [5, 7, 9, 12-18]; typically, the current of the leading phase is negative (i.e. is being sourced into the return electrode), as to depolarize neurons near the active electrode [3], while the current of the balancing phase is positive (i.e. is being sourced into the active electrode), and of equal amplitude and duration as the leading phase, as to make the stimulus charge-balanced. The key parameters of such a stimulus pattern are accordingly the pulse-width (i.e. the duration of each phase of a biphasic pulse), the pulse amplitude, and the pulse frequency (i.e. the rate at which biphasic pulses are delivered). Depending on the stimulation application and electrodes used, said stimulus parameters may vary significantly [3]. However, generally, stimulus amplitude falls between 10µA and 10mA, pulse-width between 10µs and 1ms, and pulse frequency below 300Hz.

Although the parameters of the applied current stimulus may vary widely across neural stimulation applications, when biphasic stimulus (with sufficient pulse-width and amplitude to trigger a desired level of neural modulation) is applied, high bipolar voltages (i.e. > ±10V) are often observed across the active and return electrodes due to Ohm's law and the impedance presented by Z_E. Furthermore, as illustrated by the Figure 1.2 Z_E linear-circuit-element approximation, Z_E may not just exhibit a "high" impedance (requiring high, bipolar electrode driving voltages), but may also exhibit a widely varying frequency-dependence (i.e. Z_E can display both resistive and capacitive characteristics); furthermore, Z_E has been observed to change significantly during *in-vivo* operation and after prolonged use [3, 4]. Accordingly, a

robust and practical neural stimulation system not only requires high (and bipolar) voltage compliance, but also performance that is invariant to the frequency-dependent characteristics of Z_E (within the purely resistive to purely capacitive phasor range).

To achieve (or approach) said performance, electrical neural stimulation systems have been implemented across a wide range of technologies with varying levels of integration. However, silicon bulk-CMOS technologies serve as the backbone of modern digital electronics and allow the low-cost realization of sophisticated systems incorporating both digital and analog functional blocks on a tiny, single silicon chip. Due to the resulting small form-factor and compatibility with low-power design, such single-chip bulk-CMOS solutions could be advantageous to the future development of implantable neural interfaces for BBCIs and neuroprostheses. However, the aforementioned bipolar, high-voltage compliance needed by a practical neural stimulator presents significant barriers for implementation in a modern, low-voltage bulk-CMOS technology, since the absolute terminal-to-terminal voltages of a transistor in such a process must be kept within a small window (e.g. under 1V, 2.5V, 3.3V, etc.); these limits are established by the foundry to prevent device failure (primarily gate-oxide breakdown) and to assure reliable operation over time. As a result, many neural stimulator integrated circuits (ICs) published to date are constrained in voltage compliance by these foundry ratings (e.g. a stimulator chip utilizing VDD-rated devices typically has a maximum voltage compliance of ±VDD/2).

Therefore, leveraging the form-factor and cost benefits afforded by bulk-CMOS integration (which could enable the development of smaller and more complex implantable neural interfaces) lies in opposition to the implementation of practical neural stimulation systems. Accordingly, to overcome this problematic integration barrier, this thesis presents a new, high-voltage compliant stimulator front-end (and its enabling circuits) that can be designed and fabricated using a low-voltage, CMOS process. The proposed front-end can be used to drive constant-current biphasic stimulus, with voltage compliance decoupled from the VDD-rating of the implementing transistors; instead, the voltage compliance is only restricted by the voltage limitations imposed by more voltage-tolerant structures like metal-to-metal capacitors, and, in a bulk-CMOS process, the reverse breakdown voltage of the p-substrate-to-deep-n-well junction.

This thesis is organized as follows. In Chapter 2, the state-of-the-art in "high-voltage" CMOS stimulators is discussed; specifically, previous attempts in extending the compliance of bulk-CMOS stimulators past the intrinsic limitations imposed by the VDD-rating of the

implementing transistors. Then, in Chapter 3 the proposed high-voltage compliant, bulk-CMOS-compatible neural stimulation front-end is introduced, with emphasis on the high-level H-bridge topology it employs and its critical sub-system, which uses feedback to drive stimulus current and protect front-end circuits from dangerous voltage levels. The two specialized circuits critical to the proposed integrated front-end are then discussed in Chapter 4 and Chapter 5, including the presentation of transistor-level schematics, post-layout simulations, and post-fabrication measurements. The efficacy of the proposed integrated front-end in actual stimulation applications is then discussed in Chapter 6, via the presentation of *in-vivo* experimental (rat) results using a prototype PCB-based stimulation system that emulates the functionality of the integrated front-end topology. Then, in Chapter 7, which directly precedes a brief conclusion of the thesis, an integrated circuit is presented that fully implements the proposed neural stimulation front-end in 65nm bulk-CMOS (with post-layout simulation results provided to demonstrate its high-voltage, electrode-invariant, biphasic-stimulus-driving functionality).

Chapter 2. STATE-OF-THE-ART IN HIGH-VOLTAGE CMOS STIMULATORS

To optimize different aspects of neural stimulator performance, a wide array of stimulator designs have been proposed and demonstrated in silicon. For example, to maximize stimulator efficiency, switched-capacitor-based front-ends have been proposed that employ large off-chip capacitors, which are charged with high-efficacy using specialized integrated circuits, and subsequently used to deliver stimulus by connecting said charged capacitors across the active and return electrodes [6, 9, 10]. Other stimulator designs aim at reducing the total overall form-factor by minimizing the need for large off-chip series blocking capacitors, either by assuring a high degree of charge-balance is intrinsically achieved by the stimulus-driving circuitry (therefore precluding the need to do electrode-shorting post-stimulus with series blocking capacitors in the stimulus pathway) [15] or by delivering stimulus using high-frequency, complementary current pulses driven through small, on-chip capacitors (as to emulate the fault-protection afforded by employing off-chip series blocking capacitors) [8, 19].

However, of the many integrated neural stimulation systems in the present literature, only several display high-voltage compliance while being compatible with low-voltage, bulk-CMOS integration [11-13]. Said designs employ current-regulated stimulation and have two main components. First, the high voltage supply, HVDD, which supplies the stimulus current, is generated on-chip using a switched-capacitor-based DC-DC converter. Second, a specialized stimulator front-end is used to interface said HVDD with current sources and/or the active and return electrodes, as to drive charge-balanced, current-regulated stimulus between an active and return electrode pair.

The HVDD that can be generated by the DC-DC converter isn't terribly constrained, with circuits having been previously demonstrated in bulk-CMOS technologies that can achieve NVDD generation (e.g. charge-pump, voltage-doubler, etc.), where VDD is the rating of the implementing devices and N > 3, 4, 5, and so on [20-22]. However, depending on the topology of the employed front-end, HVDD may be limited with respect to VDD, since how said HVDD stresses the current sources and switch devices used in stimulator front-end must also be considered. Accordingly, in this chapter the state-of-the-art in high-voltage compliant neural stimulation systems that have been demonstrated in low-voltage, bulk-CMOS is reviewed, with

emphasis on the front-end topology employed by each system, and how the front-end design limits HVDD relative to VDD (in terms of realizing a practical and implementable system). Additionally, other advantages and disadvantages of each topological approach are discussed.

2.1   GROUND-RETURN FRONT-END TOPOLOGY

Perhaps the most commonly used front-end topology across current-regulated neural stimulators is referred to as the "ground-return" topology. In said topology, current sources of both "source" and "sink" polarity can be connected to an active electrode via switches, and the return electrode is shorted to a low-impedance node, which is typically at the half-supply potential; accordingly, for a dual-supply system with +VDD and −VDD rails, the return potential is typically held at ground (hints the topology name). The ground-return front-end is often employed by neural stimulation systems featuring a high channel count, with each active electrode having dedicated source/sink-regulation and a single common return electrode shared by all active-return electrode pairs (with the return electrode itself typically being low-impedance) [11, 17, 18].

Figure 2.1 illustrates the operation of the ground-return front-end topology (with a bulk-CMOS implementation) when delivering biphasic, constant-current stimulus.
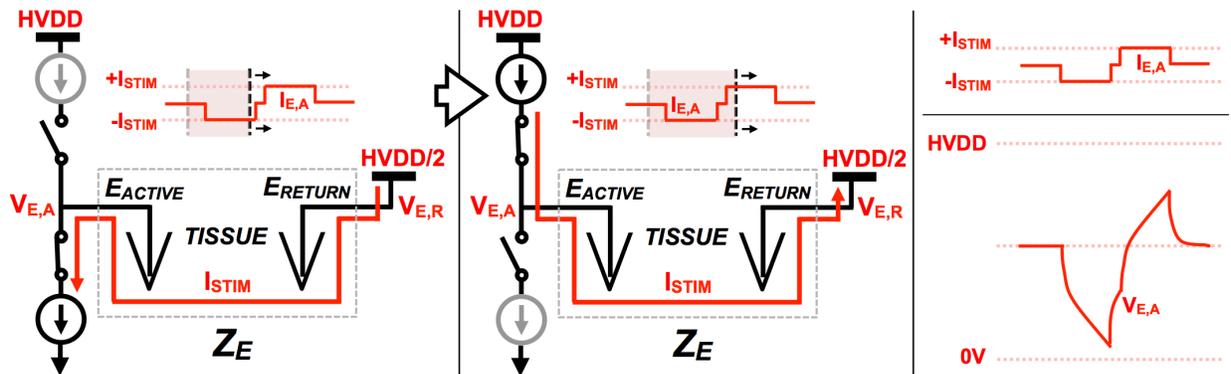
Figure 2.1. Operation of a bulk-CMOS implemented "ground-return" stimulator front-end; single-supply nature of bulk-CMOS forces "ground" to be mid-rail (HVDD/2).

As shown in Figure 2.1, during stimulus delivery the voltage at the active electrode terminal can potentially vary between 0V and HVDD. Accordingly, if standard switch and current source designs were to be used in the illustrated front-end circuit, HVDD would be constrained to VDD

(i.e. the VDD-rating of the implementing devices) and the resulting bipolar compliance would be less than ±VDD/2 (since each current source would have a non-zero dropout voltage) [17, 18].

However, by using device-stacking techniques in implementing the switches shown in Figure 2.1, a ground-return front-end design featuring twice the typical compliance (i.e. ±VDD) has been demonstrated in 65nm bulk-CMOS [11]. Yet, further extending HVDD relative to VDD is problematic with the approaches used in [11] due to challenges in implementing the source-regulating electronics, since the required source-mode current source must basically "float" with HVDD while being controlled by circuits operating between VDD and ground (as well as being well-matched to the sink-mode current source). Likewise, if the device-stacking technique used in [11] to implement the front-end switches were to be extrapolated for operation at higher HVDD-to-VDD ratios, the resulting circuits would become increasingly complex, if not impractical.

In terms of high-voltage operation, another drawback of the ground-return topology in bulk-CMOS is that it requires two positive power supplies that must be both generated and regulated. Accordingly, if HVDD were to be elevated past 2VDD, an on-chip, voltage-boosting power–converter (of likely moderate-efficiency) would be required to regulate the low-impedance node interfacing with the return electrode. Additionally, depending on the usage of large capacitors in-series with the active and/or return electrodes, the static difference between the return electrode bias and chip ground could result in DC leakage currents through the tissue, and as HVDD further increases, said leakage current could become more problematic.

2.2 Differential Front-end Topology

In a current-regulated stimulator employing a "differential" front-end topology, matched current sources of opposite source/sink polarity are simultaneously connected to active/return or return/active electrodes, via switches, to deliver charge-balanced stimulus. If both current sources are well-matched and the electronics interfacing with each electrode have the same input impedance (from the perspective of an electrode), equal and opposite (i.e. differential) voltage variation should be observed at the active and return electrode terminals during stimulus delivery. Accordingly, like other differential circuits, the common-mode of the front-end must be set; specifically, both electrodes need to be set to the half-supply voltage before stimulus delivery is commenced (if the voltage compliance of the front-end is to be maximized). A

distinct advantage provided by this front-end topology is in stimulation systems employing multiple differential front-ends, charge-balanced stimulus can be simultaneously delivered to multiple active electrodes and multiple return electrodes (as long as the total source and sink currents, at a given time, are well balanced); in-contrast, with the ground-return front-end discussed in Section 2.1, simultaneously stimulated active electrodes must share a common return electrode.

Figure 2.2 illustrates the operation of the differential front-end topology (with a bulk-CMOS implementation) when delivering biphasic, constant-current stimulus.
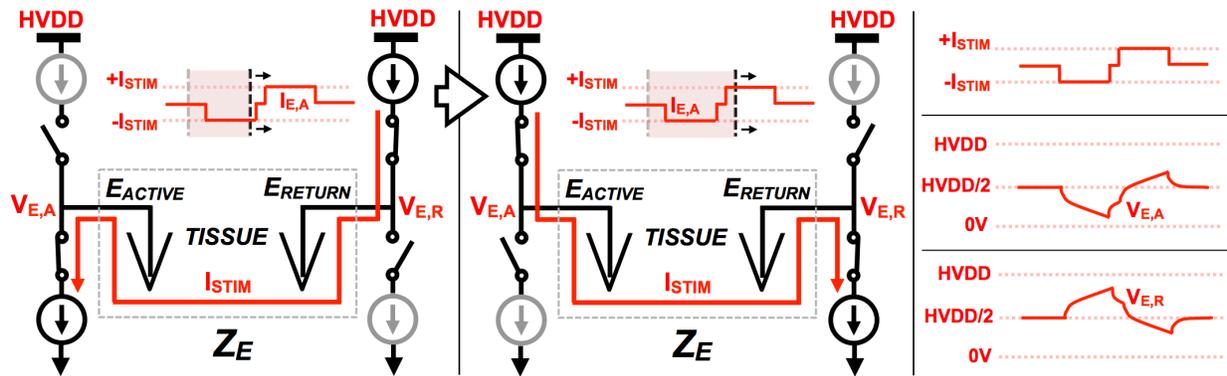
Figure 2.2. Operation of a bulk-CMOS implemented "differential" stimulator front-end; all current sources are balanced.

As shown in Figure 2.2, during stimulus delivery the voltages at both the active and return electrode terminals have the potential to vary between ground and HVDD. Accordingly, if standard switch and current source designs were to be used in the illustrated front-end circuit, HVDD would be constrained to VDD (i.e. the VDD-rating of the implementing devices) and the resulting bipolar voltage compliance would be less than ±VDD (since each current source would have a non-zero dropout voltage) [5]. Therefore, a standard differential front-end can achieve approximately twice the "intrinsic" voltage compliance of a standard ground-return front-end.

However, more specialized designs that can employ elevated HVDD levels have been developed, such as the stimulation system featured in [12], which demonstrates approximately ±6V compliance using 1V and 2.5V devices. With that said several high-voltage interfacing circuits critical to the operation of the stimulation system in [12] are not disclosed, and the closed-loop technique it employs to quasi-adiabatically set the effective HVDD and ground of the differential front-end (as well as set the switch and current-DAC control signals) may not be

able to reliably operate with resistive Z_E loading (in [12], the stimulator is only demonstrated with a very capacitive-looking Z_E, resulting in relaxed dV/dt at both electrodes during stimulation).

Accordingly, in general, a differential front-end is problematic as HVDD further increases relative to VDD (like the ground-return topology) due to the design of reliable and controllable source-mode current sources (and the corresponding pass-high switch). Furthermore, with a differential front-end a high-degree of balance is required between source and sink current sources (as well as the impedance seen by each current source) in order to assure fully differential operation (as to maximize the stimulator compliance) and prevent unpredictable common-mode variation at the electrodes; else, active common-mode setting circuits must be employed that can "absorb" said mismatch. Therefore, considering the complex circuits used in [12], designing a balanced differential front-end could become increasingly difficult as HVDD is further increased relative to VDD. Furthermore, having to establish the HVDD/2 common-mode voltage of each electrode, prior to stimulation, further contributes to the overall implementation complexity of differential stimulation front-ends for which HVDD is significantly greater than VDD.

2.3   H-BRIDGE TOPOLOGY

In delivering charge-balanced stimulus, an "H-bridge" front-end only employs current regulation of a single polarity (source or sink) and alternates the electrode (active or return) said current regulation is interfacing with while the other electrode is connected to a low-impedance node at an adequate voltage to keep the current regulation from dropping out. Figure 2.3 illustrates the operation of a sink-regulated H-bridge front-end topology (with a bulk-CMOS implementation) when delivering biphasic, constant-current stimulus. As shown in Figure 2.3, during stimulus delivery the voltages at both the active and return electrode terminals have the potential to vary between ground and HVDD. Accordingly, if standard switch and current source designs were to be used in the illustrated front-end circuit, HVDD would be constrained to VDD (i.e. the VDD-rating of the implementing devices) and the resulting bipolar voltage compliance would be less than ±VDD (since each current source would have a non-zero dropout voltage).
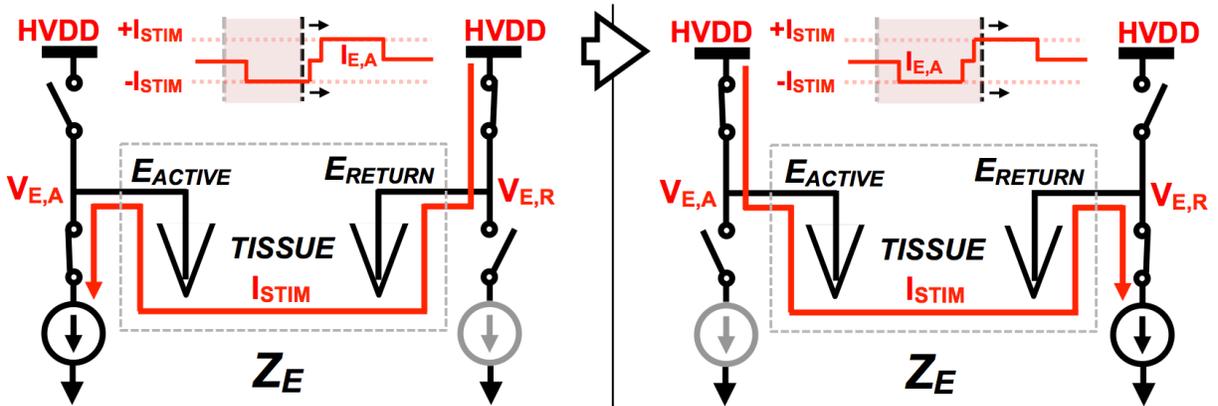
Figure 2.3. Operation of a bulk-CMOS implemented "H-bridge" stimulator front-end with sink-regulation.

Accordingly, a sink-regulated H-Bridge front-end provides advantages in realizing a high-voltage complaint stimulation system compatible with low-voltage bulk-CMOS integration, since only sink regulation is required. Therefore, some of the most problematic high-voltage implementation challenges associated with other front-end topologies (i.e. designing source-regulating electronics that can float with HVDD, be controlled by circuitry operating between ground and VDD, and have adequate performance) can be bypassed. As a demonstration of said amenability to high-voltage operation, the H-bridge stimulator featured in [13] is approximately ±9V compliant (while implemented using 3.3V bulk-CMOS devices), with the overall stimulation system having significantly lower complexity than the high-voltage, differential stimulation system featured in [12] and discussed in Section 2.2.

An H-bridge front-end may provide additional advantages with respect to stimulator performance and bulk-CMOS implementation. As shown in Figure 2.3, only one sink-regulating current source is used at a time. Therefore, a single current source could be used to deliver an entire biphasic stimulus waveform; such a design could be potentially leveraged to provide improved charge-balance performance. Secondly, unlike a ground-return front-end (Section 2.1), the H-bridge front-end illustrated in Figure 2.3 features only one power supply (HVDD); likewise, the Figure 2.3 H-bridge front-end does not require the electrode to be set to a half-rail, common-mode voltage prior to stimulus delivery (unlike a differential stimulator). Accordingly, it can be argued a sink-regulated H-bridge front-end is more suited for bulk-CMOS

implementation, as compared to the other front-end topologies discussed in this chapter, due to the truly single-supply nature of its design.

However, an H-bridge front-end also has its performance limitations. With regards to a sink-regulated H-bridge (Figure 2.3), the active electrode is only directly connected to current-regulating electronics during "negative" stimulus delivery. Accordingly, with a stimulation system employing multiple H-bridge front-end modules, each interfacing with an electrode (with each "module" being a switch to a sinking current source and switch to HVDD), charge-balanced stimulus can only be reliably driven between a single active-return electrode pair at a time. Yet, this performance restriction does not prohibitively limit the potential uses of a stimulator employing an H-bridge front-end (or multiple front-end modules), since there are many neural stimulation applications that don't require simultaneous, multi-channel stimulus delivery. Furthermore, even some high channel-count stimulation systems employing ground-return front-ends (which could potentially stimulate multiple active electrodes simultaneously) are controlled in a manner that makes it so only a single active electrode can be stimulated at a time [17] (so in general, such performance is fairly common).

Much more problematic than the inability to simultaneously stimulate through multiple channels is the performance of a bulk-CMOS-implemented, sink-regulated H-bridge front-end when Z_E looks capacitive, as illustrated in Figure 2.4.
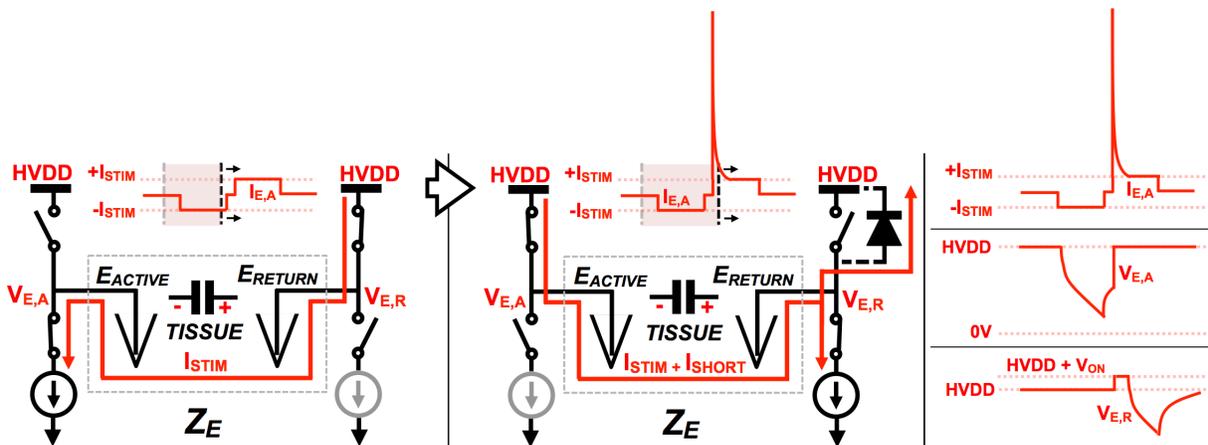
Figure 2.4. Unpredictable and unreliable performance of stimulator front-end (employing standard, sink-regulated H-bridge topology) when Z_E stores charge.

Accordingly, if Z_E holds a voltage through the interphase delay of stimulus delivery, the voltage exerted on the front-end electronics by an electrode will exceed HVDD; considering the bulk-CMOS devices that would be used to implement the components of the circuit illustrated in Figure 2.4, this "supra-HVDD" voltage, if large enough, would likely forward-bias an internal device junction (e.g. the drain-to-body junction of a PMOS device). The other side of the forward-biased junction would be at DC, and therefore the active and return electrodes would be effectively shorted, resulting in high, unregulated current through the tissue (which is undesired). Likewise, if HVDD is at its maximum possible voltage for a given process (as to maximize the compliance of the stimulator front-end), then a voltage exceeding HVDD could overstress the front-end electronics (depending on the implementation), or exceed the reverse breakdown voltage of a parasitic junction in the silicon process stack (which would also result in unregulated current through the tissue). Accordingly, as is, the H-bridge front-end shown in Figure 2.3 and Figure 2.4 can really only be used to deliver stimulus to resistive electrodes (or to electrodes for which the resistive impedance dominates), otherwise the driven stimulus current cannot be reliably regulated through the entire duration of a biphasic pulse.

It is unclear how [13] and other high-voltage compliant, bulk-CMOS implemented H-bridge stimulators address this electrode-dependent performance. Accordingly, in this thesis a novel stimulator front-end is comprehensively presented and discussed, that, while based on a sink-regulated H-bridge (so as to achieve state-of-the-art voltage compliance), is designed to specifically overcome this reliability issue and provide electrode-invariant performance.

Chapter 3. FRONT-END TOPOLOGY OVERVIEW

As discussed in Chapter 2, stimulators employing H-bridge front-ends have been previously implemented in low-voltage bulk-CMOS, and have demonstrated the ability to achieve high-voltage compliance [13], but unaddressed is the ability of such a stimulator front-end to interface with an unknown, and potentially charge-storing electrode-tissue-interface impedance (Z_E). Accordingly, in this chapter a new H-bridge stimulator front-end topology is presented which 1) is compatible with low-voltage, bulk-CMOS integration and can achieve state-of-the-art voltage compliance, and 2) performs invariantly to the resistive/capacitive characteristics of Z_E. In Section 3.1, the high-level concepts employed by said topology are first introduced, and then in Section 3.2 the actual front-end design, which can be implemented using low-voltage bulk-CMOS devices, is described in detail at the system-level. Then in Section 3.3, the positive-current driver (PCD), a key sub-system of the proposed front-end, is discussed, and the chapter is concluded with Section 3.4, which provides important implementation considerations that may be useful to a designer trying to realize the described stimulator front-end in silicon.

3.1 TOPOLOGY CONCEPTS

The unaddressed problem with a standard H-bridge stimulator topology is its compatibility with a wide range of electrode-tissue-interface impedances; specifically, capacitive looking impedances that may hold a significant voltage through the interphase delay of the biphasic stimulus. This compatibility issue stems from the fact that current-delivery has two complementary phases, during which a single supply (HVDD) is used as the low-impedance node of the H-bridge.

This issue could be potentially resolved if the electrode-tissue-interface voltage could be assured to be close to 0V before an H-bridge driver uses HVDD to supply the balancing stimulus current. A passive way to achieve this functionality would be to extend the interphase delay as long as it needs to be to allow Z_E to self-discharge. However, with many Z_E models referenced in the literature being a resistor and capacitor in-series [5-14], it would be difficult to predict how long self-discharge may take. Furthermore, Z_E is, in actuality, a non-linear impedance which can change over time (i.e. when implanted) [3, 4]. Accordingly, considering that it's typically desired to keep the interphase delay as short as possible, having its duration dependent on a time-

constant, which is electrode-dependent, time-varying, and only models the behavior of a non-linear impedance, is most likely not an acceptable solution.

Alternatively, the discharge of Z_E can be forced through active means; specifically, by using the balancing stimulus current, as shown in Figure 3.1.
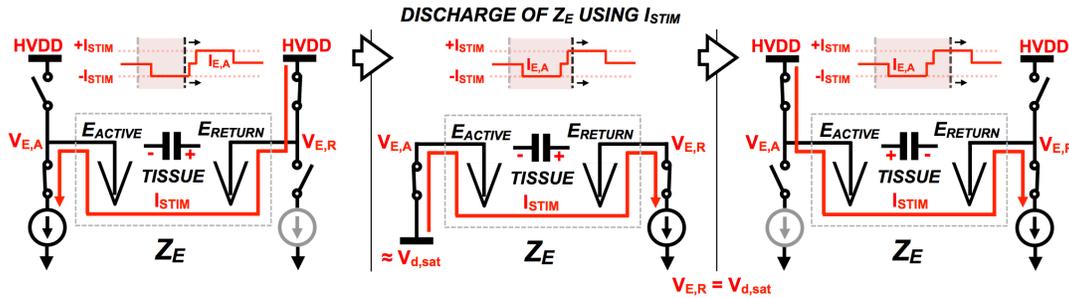
Figure 3.1. Modified H-bridge topology; balancing stimulus is supplied by Z_E (with other side connected to low-voltage, low-impedance node) before HVDD is used to supply balancing current.

In Figure 3.1, the leading stimulus pulse is driven through Z_E the same way as with a typical sink-regulated H-bridge, resulting in negative I_{STIM} through the active electrode (E_{ACTIVE}). In this initial configuration, HVDD, which is connected to the return electrode (E_{RETURN}), provides the low-impedance node, and a sinking current source, with a dropout voltage of $V_{d,sat}$, regulates I_{STIM} through Z_E. Then, after the interphase delay, balancing-pulse delivery is broken up into two sub-phases. During the first sub-phase, a low-voltage power rail, approximately equal to the current source $V_{d,sat}$, is connected to the active electrode and Z_E is discharged via I_{STIM}. As a result, balancing stimulus is delivered (i.e. positive I_{STIM} through the active electrode) while the voltage across Z_E is brought down towards 0V.

When the voltage across Z_E finally falls to the $V_{d,sat}$ of the current source, HVDD is connected to the active electrode and used as low-impedance node of the H-bridge, resulting in the continued delivery of positive I_{STIM} to the active electrode, without interruption; this second sub-phase configuration is then maintained for the remainder of balancing-pulse delivery. Accordingly, regardless of the charge-storage characteristics of Z_E, a stimulator front-end using the Figure 3.1 topology concepts could potentially approach $\pm$(HVDD - $V_{d,sat}$) compliance.

However, there exist non-trivial challenges in designing an integrated stimulator (using a low-voltage bulk-CMOS process) that implements the Figure 3.1 scheme. Specifically, the

HVDD generating circuitry and the interfacing functional blocks (i.e. switches and current sources) must be designed in a way that protects individual transistors from seeing terminal-to-terminal voltages exceeding the foundry-defined voltage ratings. Additionally, the circuits and control scheme needed to force the transition between the two sub-phases of balancing-stimulus delivery must be implemented.

The remainder of this chapter will introduce a novel stimulator front-end design, compatible with low-voltage, bulk-CMOS integration, which addresses and overcomes these implementation obstacles.

3.2   LOW-VOLTAGE, BULK-CMOS-COMPATIBLE STIMULATOR FRONT-END EMPLOYING MODIFIED H-BRIDGE TOPOLOGY

3.2.1   Overview

Figure 3.2 shows a high-level schematic of the proposed stimulator front-end, which is designed to drive biphasic constant-current stimulus between two electrodes, and incorporates the active discharge of the electrode-tissue-interface impedance (Z_E) into stimulus delivery to account for Z_E charge storage. In Figure 3.2a, the general schematic is given, while in Figure 3.2b the same is shown but with the actual switch-implementation used in this work. Like with other H-bridge-style front-end topologies, Z_E is treated as a two-port load, with each port being a connection to an electrode (electrode 0 and electrode 1).
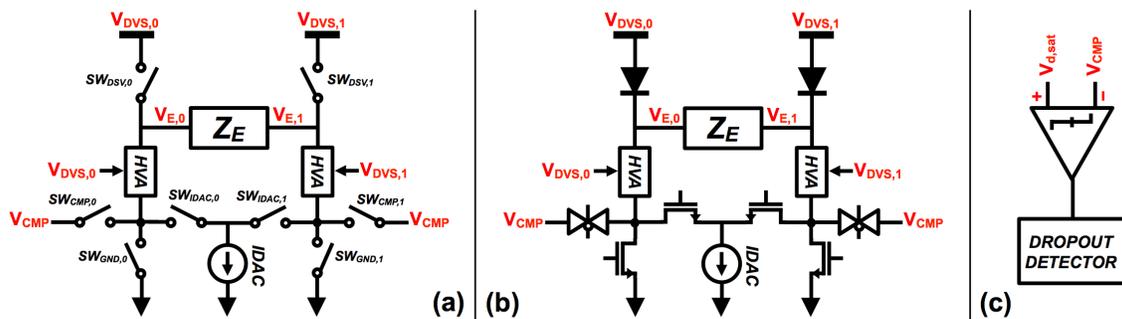
Figure 3.2. Proposed high-voltage compliant front-end (for constant-current, biphasic neural stimulation); (a) general implementation; (b) implementation used in this work; (c) comparator for current-DAC dropout detection.

3.2.1.1   Generating High Voltages

The front-end features two independently controlled dynamic voltage supplies (DVSs): one which sets $V_{DVS,0}$ and can be connected to electrode 0 via switch $SW_{DVS,0}$; and one which sets $V_{DVS,1}$ and can be connected to electrode 1 via switch $SW_{DVS,1}$. Working within a positive-current driver (PCD), a closed-loop sub-system discussed in detail in Section 3.3, each DVS can be used to supply the stimulus current across a 0V to V_{MAX} output range; for this operation, the PCD controlling the DVS would be in its SUPPLY configuration. When unloaded (i.e. when the respective SW_{DVS} switch is open), a secondary function of each DVS is to track the voltage of the electrode that is on the same side of the H-bridge; this operation is controlled by a PCD in its TRACK configuration.

3.2.1.2   Interfacing Low-Voltage Circuits with High-Voltage Electrodes

The high-voltage adapters (HVAs) effectively function as conducting, high-voltage-tolerant NMOS devices (with gates biased to a low-voltage), and accordingly protect the "low-side" circuits (switches and current-DAC) from potentially high electrode voltages while allowing these same circuits to interface with the electrodes. Each HVA requires a bias voltage, and this input is high-impedance. As is discussed in Chapter 5, for an HVA to function properly, it is important that this bias voltage is approximately equal to the voltage of the electrode the HVA interfaces with. Accordingly, each HVA is provided this bias input from the DVS on the same side of the H-bridge, which is kept at the same voltage (approximately) as the electrode throughout stimulus delivery via PCD operation.

3.2.1.3   Stimulus Current Regulation

Regulating the entire biphasic constant-current waveform is a single, sink-regulating current-DAC (IDAC). Because the IDAC sits at the "low-side" of the HVAs, the design used to implement it does not need to be high-voltage tolerant or particularly specialized (i.e. standard IDAC topologies can be used).

3.2.1.4   Switches and Comparator

As shown in Figure 3.2a and Figure 3.2b, each electrode, via an HVA, can be connected to the IDAC, ground (GND), or to a shared comparator (CMP) by properly configuring the corresponding SW_{IDAC}, SW_{GND}, and SW_{CMP} "low-side" switches; accordingly, each side has a

dedicated low-side switch set, comprised of the said three switch types. The shared comparator, shown in Figure 3.2c, is used during stimulus delivery (specifically during the discharge of Z_E via the stimulus current) to detect when the IDAC voltage falls under the IDAC dropout voltage ($V_{d,sat}$). Like the IDAC, no special voltage precautions need to be taken in implementing these switches, or the comparator, since all interface with the voltage-protected, low-side of an HVA.

The "high-side" switches ($SW_{DVS,0}$ and $SW_{DVS,1}$) directly interface with the electrodes, which may be at high voltages, and therefore the implementation of these switches is non-trivial. However, when a given electrode is at a high-voltage, a PCD will be forcing the corresponding DVS voltage to an approximately equal level, resulting in a low-voltage ($\leq$VDD) across the associated high-side switch; this can give the designer flexibility in the way the high-side switches are implemented. However, in this particular work, for simplicity and robustness, diodes (with the n-terminal connected to the electrode) are used as $SW_{DVS,0}$ and $SW_{DVS,1}$, with ON/OFF functionality provided by the PCD-controlled operation of the DVSs (see Section 3.3).

In summary, the proposed stimulator front-end requires the use of only two specialized circuits (DVSs and HVAs), with all other functionality provided by circuits that can be implemented using standard, low-voltage topologies. As it turns out, the DVS is a switched-based structure (see Chapter 4), and the HVA is a fairly passive circuit that mainly relies on the operation of the DVS in feedback to protect the low-side circuits from potentially high electrode voltages (see Chapter 5). Considering the implementation of these "specialized" blocks and that the remainder of the front-end is made up of switches, digital circuits can be used to directly control most, if not all, of the Figure 3.2 driver. Accordingly, a state-machine can be used to guide the proposed front-end through the required configurations to result in biphasic, constant-current stimulation; these configurations (or states) and the sequence of their activation are discussed next.

3.2.2   *Stimulation State-Cycle*

Before steering biphasic, constant-current stimulus between electrodes 0 and 1, the "active" electrode and the "return" electrode must be designated. In this work, the "active" electrode is defined as the electrode that sees negative stimulus current (positive current being drawn out of the electrode) during the leading pulse, and positive stimulus current (postive current being sourced into the electrode) during the balancing pulse, while the "return" electrode sees the

opposite current polarity. Because the Figure 3.2 front-end is symmetrical across Z_E and mostly digitally controlled, the electrodes 0/1 can be easily configured (and reconfigured on-the-fly) as active/return or return/active.

With electrode 0 designated as the active electrode (and electrode 1 as the return), Figure 3.3 illustrates how the Figure 3.2 front-end is guided through a specific sequence of "states" (with each state having a different front-end configuration) to drive biphasic, constant-current stimulus through Z_E. The states illustrated in Figure 3.3 are summarized as follows.
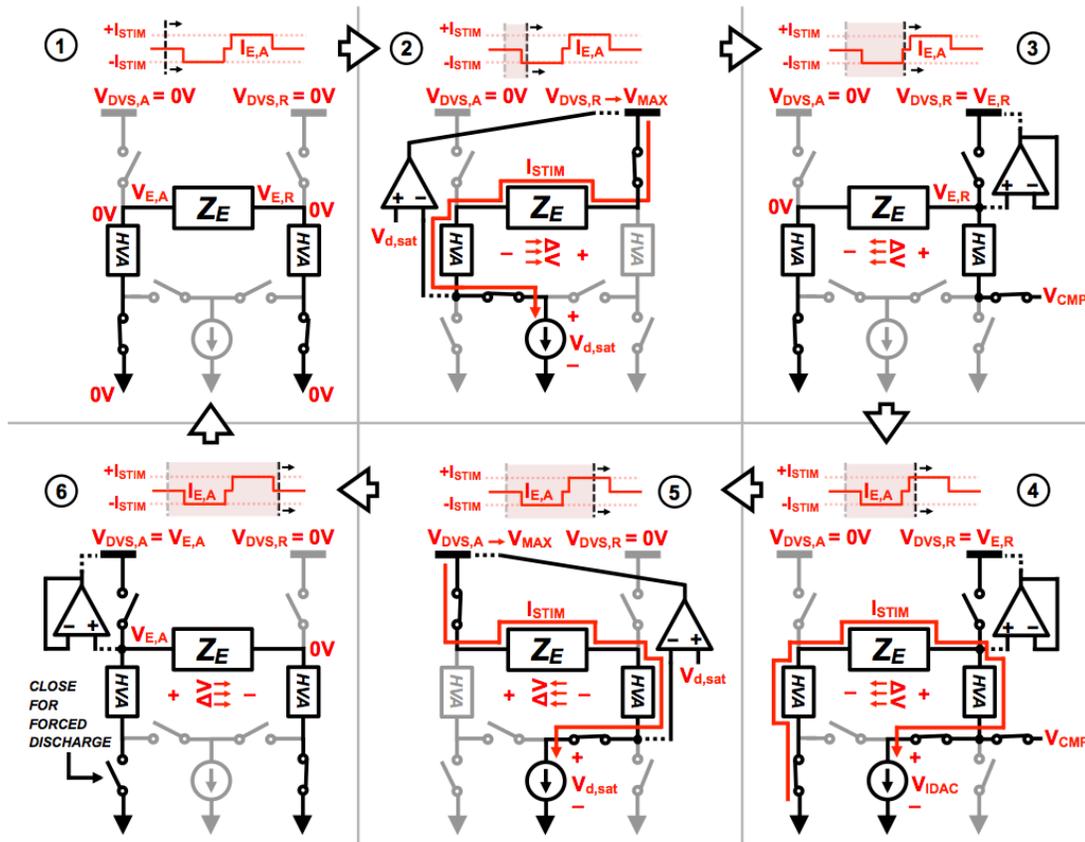
Figure 3.3. State-cycle of proposed biphasic, constant-current stimulator front-end; electrodes "0" and "1" (Figure 3.2) have been designated as "active" and "return," respectively; $SW_{CMP,0}$ and $SW_{CMP,1}$ (now $SW_{CMP,A}$ and $SW_{CMP,R}$, respectively) are only visible when closed.

3.2.2.1   State 1 - Idle

Both DVSs are inactive (as well as corresponding PCDs) and have fully discharged outputs, while the electrodes are shorted to chip ground (0V). Since neither DVS is being actively controlled, the power consumption associated with this state should be low. Furthermore, since

both DVSs are discharged to 0V (the same voltage as the electrodes) there should be little DC leakage into the tissue. In an alternative configuration, just one electrode is shorted to 0V (i.e. the return), while the other electrode see high-impedance (high-Z); in this alternative configuration the DVSs still remain discharged and inactive.

3.2.2.2   State 2 - Negative Stimulus via Return PCD

The IDAC is connected to the active-side of the H-bridge, the return DVS is connected to the return electrode, and the return PCD is activated in its SUPPLY configuration (modeled by the op-amp in the second frame of Figure 3.3). As a result, negative I_{STIM} is seen by the active electrode while the return DVS sets the return electrode voltage, as needed, to keep the IDAC voltage at the IDAC dropout voltage, $V_{d,sat}$ (as to maximize the stimulator compliance); assuming a low-headroom IDAC design is used, $V_{d,sat}$ should be no higher than a few hundred millivolts.

3.2.2.3   State 3 - Interphase Delay

This state should have a short duration (but still requires inclusion), and begins after the completed delivery of the leading pulse of the biphasic stimulus. Except for $SW_{CMP,R}$, which connects the low-side of the return HVA to the high-impedance, negative input of the comparator in Figure 3.2c, all switches on the return-side of the H-bridge are open. Accordingly, looking into the return-side of the H-bridge, the return electrode sees high-impedance. To keep Z_E from floating, the active electrode (via the active HVA) is connected to ground.

If Z_E exhibits capacitive characteristics, a significant fraction of the voltage developed across Z_E by the end of the previous state (which may be significantly higher than VDD) may be maintained across Z_E during this state. Additionally, the $-\Delta V_{d,sat}$ applied to the active electrode at the State 2 to State 3 transition will result in a negative voltage shift at the return electrode, and the return electrode voltage may decrease during the interphase delay due to Z_E self-discharge. Accordingly, the return PCD is placed in its TRACK configuration (modeled by op-amp in third frame of Figure 3.3), forcing the return DVS to track a potentially falling $V_{E,R}$ (i.e. $dV_{E,R}/dt \leq 0$). This action primarily keeps the return HVA properly biased (i.e. keeps $V_{DVS,R} \approx V_{E,R}$), but also keeps the voltage across $SW_{DVS,R}$ approximately zero, which may be important, in terms of device reliability, depending on the implementation of said switch.

The comparator is connected during this state to allow its input capacitance to equalize with the voltage at the low-side of the return HVA, so that, if needed, the dropout of the IDAC can be detected right as State 4 begins (i.e. if Z_E is mostly resistive). Accordingly, the comparator is being "primed" for a decision to-be-made in the next state, while being effectively disabled, with the comparator output ignored by an inactive dropout detection block (see Figure 3.2c).

3.2.2.4   State 4 - Positive Stimulus via Z_E Discharge

The same configuration utilized in the previous state is maintained, except the return electrode, via the return HVA, is connected to the IDAC (in addition to being connected to the dropout detecting comparator).

As the IDAC discharges Z_E via sinking I_{STIM}, the return electrode voltage falls (as the return DVS tracks it) and the active electrode sees positive I_{STIM}. Accordingly, at some point during this state the return electrode voltage, and therefore the IDAC voltage, will approach the $V_{d,sat}$ of the IDAC. But at the point of dropout, the 0 to 1 transition at the output of the comparator triggers the active dropout detector, which forces the front-end to transition to the configuration of the next state.

3.2.2.5   State 5 - Positive Stimulus via Active PCD

The remainder of the balancing pulse is delivered by disconnecting ground from the active electrode, connecting the active DVS (initially at 0V) to the active electrode, and placing the active PCD in its SUPPLY configuration. Accordingly, complementary to the State 2 front-end configuration, the IDAC regulates positive I_{STIM} through the active electrode while the active DVS supplies the stimulus current and has its voltage increased to keep the IDAC voltage at $V_{d,sat}$.

3.2.2.6   State 6 - Z_E Discharge

Due to a non-linear Z_E and/or Z_E having both capacitive and faradaic transduction mechanisms, a non-zero voltage may exist across Z_E after well-balanced biphasic stimulus has been successfully delivered. This residual charge can either be allowed to passively discharge using the configuration shown in sixth frame of Figure 3.3, or, with a slightly modified configuration, be forced to discharge by connecting the active electrode (via the active HVA) to ground. In either case the active PCD is placed in its TRACK configuration, to force the active DVS to track the

active electrode back down to 0V. Once Z_E is fully discharged, the driver can be returned to the State 1 (Idle) configuration.

If a charge-balanced waveform has already been delivered and no blocking capacitors are used, then "passive discharge" must be employed to assure charge balance is maintained (without the application of auxiliary charge-balancing circuitry). However, if a blocking capacitor does exist in the stimulus path, then the "forced discharge" method can be readily employed, and the time-constant/magnitude of the discharge current can be modified, if desired, by adjusting the resistance of the switch connecting the active electrode to ground.

3.3   POSITIVE-CURRENT DRIVER (PCD) SUB-SYSTEM

3.3.1   *Overview*

In delivering biphasic constant-current stimulus, the proposed H-bridge front-end utilizes the coordinated operation of two positive-current driver (PCD) sub-systems, each controlling the output voltage of a dedicated dynamic voltage supply (DVS). The "PCD" nomenclature is used because the primary function of the sub-system is to drive positive stimulus current into its associated electrode. Additionally, the alternate function of a PCD is to force its associated DVS to track the falling voltage of the same electrode, when no stimulus is supplied, so that all nodes within the PCD can be safely returned to low voltages. PCD_0 sets $V_{DVS,0}$ and PCD_1 sets $V_{DVS,1}$. Figure 3.4 provides a simplified schematic of $PCD_{0/1}$ (note subscripts in figure). Key blocks and concepts employed by a PCD include the following.

Figure 3.4. Positive-current driver (PCD) block diagram; subscript notation donates association with $PCD_{0/1}$.

3.3.1.1   Dynamic Voltage Supply (DVS)

The DVS is the most critical block of a PCD. A DVS is used to supply stimulus current across a voltage range of 0V to V_{MAX}. When unloaded (i.e. when the switch at the DVS output is open) the DVS is used to track the potentially falling voltage of the electrode that lies on the same side of the H-bridge.

Internally, the DVS utilizes switched-capacitor operation, and variable voltage is achieved at its output by being able to source and sink switched-capacitor current to an output capacitor. The SOURCE/SINK control bit ("SRC" used for brevity in the Figure 3.4 illustration) sets the direction in which switched-capacitor current flows through the DVS, and the drive strength of the DVS is set by the frequency of the input pulse signal, Φ, which must be transformed to complementary pulse signals Φ_A and Φ_B before being used to directly drive the DVS. As the frequency of Φ is increased (within a range the DVS is designed for), quanta of charge move through the DVS at a higher rate, resulting in higher switched-capacitor current. When loaded by a constant-current and placed in its SOURCE setting, a DVS can be modeled as having a linear relationship (with negative slope) between output voltage (average output voltage) and the period (average period) of Φ. When unloaded and in the SINK setting, the output of a DVS can be discharged in a controlled fashion (to as low as 0V), with each pulse of Φ producing a small $-\Delta V$ at the DVS output. The DVS is discussed, in detail, in Chapter 4.

3.3.1.2   High-Voltage Adapter (HVA)

An HVA effectively functions as a high-voltage-tolerant NMOS device, with its gate biased to a low-voltage. Accordingly, the voltage at the functional source of an HVA (the "low-side" terminal) is voltage-limited, and cannot exceed the functional gate voltage minus a threshold voltage (which are collectively set so that said difference is less than the VDD-rating of the low-side circuits), even if the functional drain of the HVA (the "high-side" terminal, connected to the electrode) is at a high voltage. To function in this capacity, an HVA requires a bias voltage approximately equal to the voltage at its high-side terminal (i.e. the electrode voltage). Accordingly, an HVA is biased by the DVS on the same side of the H-bridge; HVA loading to the DVS is capacitive, and is small enough to negligibly load the DVS.

Although two HVAs exist in the Figure 3.2 front-end schematic (Section 3.2.1), only one HVA is visible in the PCD block diagram (Figure 3.4). For PCD$_{0/1}$, this visible HVA is

designated as $HVA_{1/0}$ (since it's connected to the 1/0 electrode) and can be thought of as the "low-voltage" HVA of the PCD since it doesn't see high voltages at its high-side terminal when the PCD is placed in either of its feedback configurations. In contrast, the non-visible HVA in Figure 3.4, which has its high-side terminal and bias input connected to the output of the visible DVS, is designated as $HVA_{0/1}$ (since it's connected to the 0/1 electrode), and can be thought of as the "high-voltage" HVA of the PCD.

3.3.1.3 Error Signal Generation and Pulse-Gating

When a PCD is activated, closed-loop feedback is utilized to set the output voltage of its associated DVS; the error signal used to close the loop is generated by one of the comparators visible in Figure 3.4. The ε_{SUPPLY} generating comparator is used to compare the detected IDAC voltage to the desired IDAC voltage (i.e. $V_{d,sat}$, the IDAC dropout voltage). This comparator is shared by both PCDs (only one PCD is active at a time). Furthermore, this comparator can also serve as the dropout detecting comparator discussed in Section 3.2, since ε_{SUPPLY}-driven PCD feedback is not used when dropout detection is required.

The ε_{TRACK} generating comparator uses two identical capacitive dividers to compare the DVS output voltage to the voltage of the electrode that is on the same side of the H-bridge, and the capacitive dividers have sufficient division ratios to protect the comparator inputs from voltages exceeding VDD. The divided down DVS and electrode voltages are being measured from high-impedance nodes, and therefore, these critical sense signals may be sensitive to charge-injection and capacitive feed-through. Accordingly, each PCD has a dedicated ε_{TRACK} generating comparator, as to avoid the use of switches that would otherwise link the divider nodes of two PCDs if a shared ε_{TRACK} generating comparator was instead employed.

Before (or after) the H-bridge front-end has completed the Figure 3.3 stimulus delivery state-cycle (Section 3.2.2), the capacitive divider of each PCD should be reset, so that each can be forced to known (and identical) operating points between stimulus delivery events. For a given PCD, the capacitor dividers are reset by 1) closing the switch attached to the internal node of each divider (forcing the internal nodes to ground), 2) connecting the electrode to ground (via low-side switch and $HVA_{0/1}$ for $PCD_{0/1}$), and 3) discharging the DVS to 0V by placing it in its SINK setting and forwarding pulses to it; this reset can be applied to both PCDs at some point during State 1 (the "idle" state), covered in Section 3.2.2.

The output of either comparator (ε_{SUPPLY} or ε_{TRACK} generating) can be used by the PCD to gate pulses of the f_{DVS} clock signal, with the resulting signal being Φ, the pulse signal that is forwarded to the DVS. The error signal that is used as the pulse-gating signal depends on the configuration the PCD is placed in.

3.3.1.4   Low-Side Switches

For $PCD_{0/1}$, which controls $V_{DVS,0/1}$, the switches interfacing the low-side of $HVA_{1/0}$ to ground and the IDAC correspond $SW_{GND,1/0}$ and $SW_{IDAC,1/0}$ in Figure 3.2 (Section 3.2.1), respectively. If the dropout detecting comparator is also used as the ε_{SUPPLY} generating comparator, then the switch to the comparator at the low-side of $HVA_{1/0}$ in Figure 3.4 corresponds to $SW_{CMP,1/0}$ in Figure 3.2. The HVAs protect these switches (and the circuits each connect to) from high electrode voltages during stimulus delivery.

3.3.1.5   High-Side Switch

For $PCD_{0/1}$ the switch connecting the output of the associated DVS to Z_E corresponds to $SW_{DVS,0/1}$ in Figure 3.2 (Section 3.2.1). For simplicity and reliable ON/OFF operation, the high-side switch of each PCD is implemented using a diode (with the n-terminal connected to the electrode), and ON/OFF functionality is achieved by placing the PCD in feedback, as is discussed next in Section 3.3.2 and Section 3.3.3.

3.3.2   *PCD in SUPPLY Configuration*

When placed in the SUPPLY configuration (Figure 3.5), a PCD sets the output voltage of the DVS to keep the voltage across the IDAC approximately equal to a desired set voltage (i.e. $V_{d,sat}$) as the IDAC regulates I_{STIM} through Z_E. As the DVS supplies positive I_{STIM} to the electrode on the same side of the H-bridge, the DVS will have its output voltage ($V_{DVS,0/1}$) set high enough (with respect to $V_{E,0/1}$) to turn the high-side switch (a diode) ON.
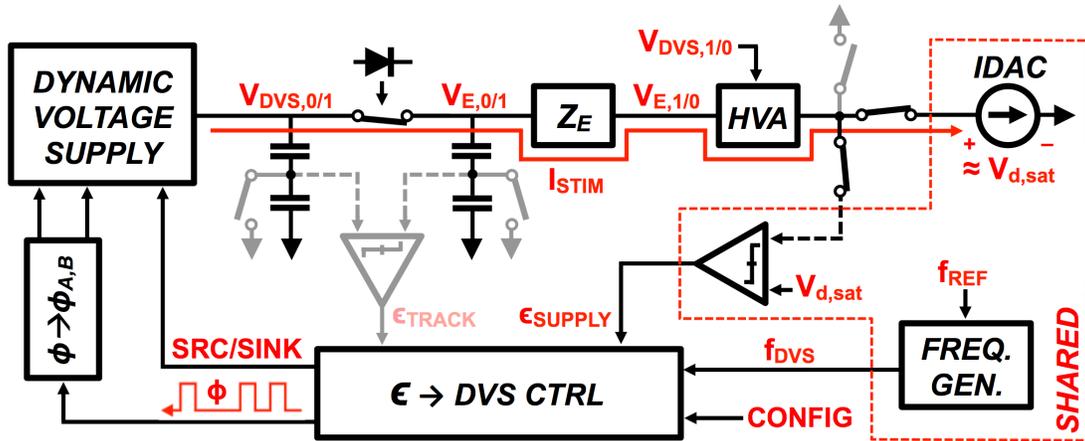
Figure 3.5. Block diagram of $PCD_{0/1}$ in SUPPLY feedback configuration.

It is known that the load current (I_{STIM}) of the DVS will be constant-current and sinking while the PCD is in this configuration, and to maintain a given output voltage the switched-capacitor-based DVS will have to supply an offsetting average current. Furthermore, by assuming the reactive component of Z_E appears capacitive, the voltage measured across Z_E (i.e. $V_{E,0/1} - V_{E,1/0}$ in Figure 3.5) can be assumed to have a derivative (with respect to time) greater or equal to zero (since I_{STIM} is constant-current). Accordingly, the DVS can be kept in its SOURCE setting while in this configuration and f_{DVS} pulses can be gated using ε_{SUPPLY}, as to produce a Φ which has an average period that sets $V_{DVS,0/1}$ to the required level to keep the IDAC voltage at the $V_{d,sat}$ set voltage (on average). This ON/OFF DVS regulation scheme prevents instability within the PCD loop; however, there will be voltage ripple at the DVS output (and subsequently at both electrodes) of predictable and limited magnitude due to the switched-capacitor nature of the DVS and the ON/OFF DVS conduction cycles.

For the DVS to deliver I_{STIM} across its full output voltage range, the frequency of the pre-gated pulse signal (f_{DVS}) must be made sufficiently high for the maximum output power condition (i.e. delivering I_{STIM} at V_{MAX}).

3.3.3 *PCD in TRACK Configuration*

When placed in the TRACK configuration (Figure 3.6), the PCD is not delivering stimulus to Z_E and its associated DVS is unloaded. Meanwhile, on the other side of the H-bridge the low-side of the HVA is set to ground (see Figure 3.3 state-cycle in Section 3.2.2). Accordingly, the Figure 3.6 configuration is needed to force $V_{DVS,0/1}$ to be approximately equal to $V_{E,0/1}$, as to keep the

high-side switch (a diode) reliably OFF and to keep $HVA_{0/1}$ biased properly (since $V_{E,0/1}$ may be at any level in the 0V to V_{MAX} range).

Figure 3.6. Block diagram of $PCD_{0/1}$ in TRACK feedback configuration.

The error signal used to enable this closed-loop operation is a quantized version of the difference signal $V_{DVS,0/1} - V_{E,0/1}$. Since these voltages may be both high, each are accessed using capacitive dividers. Assuming the reactive component of Z_E looks capacitive, it can be safely assumed that when placed in this feedback configuration (according to when the TRACK configuration is used, for either PCD, in the Figure 3.3 state-cycle) the voltage across Z_E (equal to $V_{E,0/1}$ in Figure 3.6) can only move in one direction: down, towards 0V. Accordingly, the DVS can be kept in its SINK setting while the PCD is in this configuration, and the ε_{TRACK} generating comparator can be used for error quantization. The resulting 1-bit error signal, ε_{TRACK}, is used to gate pules into the DVS, with each forwarded pulse resulting in a $-\Delta V$ at the DVS output, and pulses are forwarded to the DVS until its output has fallen to (or slightly below) the electrode voltage.

For a given DVS design, the maximum rate of DVS discharge is limited by f_{DVS} in Figure 3.6 (i.e. the frequency of the pre-gated clock signal, f_{DVS}). Accordingly, when a PCD is in the TRACK configuration, f_{DVS} should be made sufficiently high to have $V_{DVS,0/1}$ be able to track a worst-case change in $V_{E,0/1}$.

3.3.4 *Pulse-Gating Circuit*

Figure 3.7 shows a circuit proposed for f_{DVS} pulse-gating, with its design assuring that if the pulse-gating signal (PGS) is high (signaling the DVS should be ON) at the negative edge of f_{DVS}, the next f_{DVS} period (beginning with the rising edge) will be forwarded in its entirety; likewise, if the PGS is low, f_{DVS}, over the same interval, will not be forwarded.
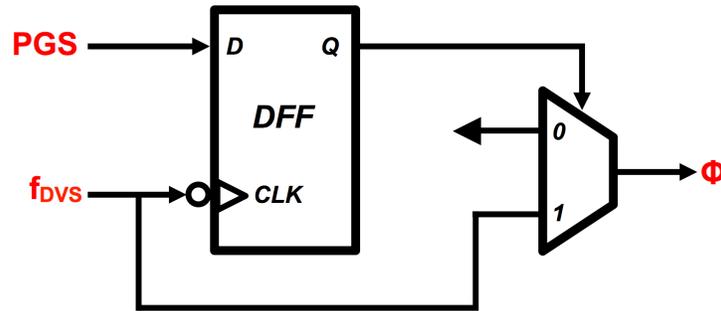
Figure 3.7. Pulse-gating circuit proposed for use by PCDs.

Accordingly, ignoring negligibly small static gate-delays, the circuit has two delay components: 1) the static $1/(2f_{DVS})$ delay between the pulse-gating circuit decision and the time at which the rising edge of the forwarded f_{DVS} pulse exits the pulse-gating circuit; and 2) the delay between the PGS signal arriving at the pulse-gating circuit and the time in which the pulse-gating decision is made, with said delay falling between zero and $1/f_{DVS}$, depending on the arrival of the PGS signal relative to the negative edge of f_{DVS}. This is just one possible pulse-gating circuit, and it's likely that other designs could be used, possibly with improved delay performance.

3.3.5 *Summary of Digitally Set PCD Configurations*

The configuration a PCD is placed in (e.g. SUPPLY, TRACK) determines: 1) if the dedicated ε_{TRACK} generating comparator (CMP) of the PCD is enabled; 2) which signal is used to gate f_{DVS} pulses into the DVS (e.g. ε_{SUPPLY} or ε_{TRACK}); 3) which SOURCE/SINK setting the DVS remains fixed in; and 4) whether the capacitive divider reset switches are opened or closed. Furthermore, assuming f_{DVS} can be changed (or multiplexed from a selection of clocks), then each configuration can be provided a tailored f_{DVS} frequency (for a given configuration, it may be useful to run the DVS at a lower maximum frequency than in others). Table 3.1 provides a

summary of said settings for the different PCD configurations. If the pulse-gating signal (PGS) is high, pulses are forwarded to the DVS. The capacitive divider reset switches are active-high (i.e. NMOS switches).

Table 3.1. Positive-Current Driver (PCD) Configuration Summary

Configuration #	Description	$\varepsilon \rightarrow$ DVS CTRL			ε_{TRACK} CMP EN	CAP DIV RESET
		PGS	SOURCE /SINK (0/1)	f_{DVS}		
0	IDLE	0	0	0 (DC)	NO	0
1	SUPPLY	ε_{SUPPLY}	0	$f_{DVS(1)}$	NO	0
2	TRACK	ε_{TRACK}	1	$f_{DVS(2)}$	YES	0
3	BLEED DOWN	1	1	$f_{DVS(3)}$	NO	0
4	DISCHARGE/RESET	1	1	$f_{DVS(4)}$	NO	1

However, as shown Figure 3.3 (Section 3.2.2), in order for biphasic, constant-current stimulus to be delivered to Z_E, coordination must exist between the configurations of a PCD and the ON/OFF settings of the low-side switch sets. Furthermore, an HVA has its own set of possible configurations, and at different points during biphasic stimulus delivery the configuration of an HVA must be changed. Accordingly, in terms of the Figure 3.3 stimulation state-cycle, each front-end configuration shown is really the culmination of properly setting the configurations of the two PCDs, two low-side switch sets, and two HVAs; the configurations of an HVA and low-side switch set are discussed in Chapter 5.

The SUPPLY and TRACK configurations of a PCD (as well the expected simultaneous low-side switch set configurations) have already been described, in detail, in Section 3.3.2 and Section 3.3.3, respectively. The remaining PCD configurations, as listed in Table 3.1, are IDLE, BLEED DOWN, and DISCHARGE/REST.

In the IDLE configuration, a PCD is essentially powered down; no pulses are forwarded to the DVS, the ε_{TRACK} generating CMP is disabled, the SOURCE/SINK setting is arbitrarily set to SOURCE, and if the other PCD is not using the ε_{SUPPLY} generating CMP, then the shared comparator may also be disabled (i.e. depends on the state/configuration of the overall stimulator). During stimulus delivery, the IDLE configuration can be used as a low-power

configuration when a PCD doesn't need to be in the SUPPLY or TRACK configuration. Accordingly, when in IDLE it's still important for the capacitive dividers to be functional (i.e. have the reset switches kept open), since the voltage at the electrode associated with the capacitive divider is not known and can vary due to the operation of the other PCD. However, when $PCD_{0/1}$ is placed in IDLE it is assumed $V_{DVS,0/1}$ and $V_{E,0/1}$ are both low (e.g. 0V to approximately $V_{d,sat}$); as long as this condition is met, the IDLE configuration requires no specific low-side switch set configuration, on either side of the H-bridge.

The BLEED DOWN configuration is identical to IDLE, except the DVS output is discharged in open loop (i.e. the DVS is fixed in the SINK setting with all f_{DVS} pulses forwarded through to Φ). Although this configuration isn't critical to the operation of a PCD or the biphasic front-end as a whole, it's useful in providing extra assurance the $PCD_{0/1}$ high-side switch diode stays reliably off after $PCD_{0/1}$ has returned $V_{DVS,0/1}$ back down to $V_{d,sat}$ (via tracking $V_{E,0/1}$ during State 3 and State 4 of the Figure 3.3 state-cycle). With that said, even if the high-side switch diode does turn on and conduct after such has occurred, the current through Z_E should be virtually unaffected; accordingly BLEED DOWN is very much an optional PCD configuration, and the IDLE configuration can likely be used interchangeably.

The DISCHARGE/RESET configuration of a PCD is like BLEED DOWN, except 1) the reset switches of the capacitive dividers are both closed and 2) it's assumed that the electrode associated with the capacitive divider is set to 0V (via the low-side switch to ground and the HVA connected to said electrode). Accordingly, after a short interval of time has passed while in this configuration, $V_{E,0/1}$, $V_{DVS,0/1}$, and the capacitive divider outputs will all be at 0V, and the capacitive dividers will be ready to be used again by $PCD_{0/1}$ for electrode tracking. Accordingly, like IDLE and BLEEDOWN, this configuration should only be activated when the electrode and DVS voltages associated with the capacitive divider of the PCD are known to be low, which is not a problem since the purpose of this configuration is the prepare a PCD for stimulus delivery (and therefore is only activated either after or right before the front-end has progressed through a stimulation state-cycle).

3.4   ADDITIONAL IMPLEMENTATION NOTES AND CONSIDERATIONS

3.4.1   *Voltage Compliance*

Since the biphasic driver front-end employs the constant-current discharge of Z_E during balancing-pulse delivery, the proposed integrated stimulation front-end has a bipolar compliance of $\pm V_{COMP,PCD}$, where $V_{COMP,PCD}$ is the compliance of a PCD when driving a monophasic stimulus pulse. Ideally, $V_{COMP,PCD}$ would be the maximum output voltage of the DVS (V_{MAX}) minus the dropout voltage of the IDAC ($V_{d,sat}$). However, in the proposed front-end implementation (Figure 3.2b in Section 3.2), each high-side switch is a diode, with a turn-on voltage of V_D at I_{STIM}. Accordingly, assuming the HVA in the stimulus current path (for a SUPPLY-configured PCD) is very conductive (and accordingly has a small voltage drop across it), the biphasic compliance of the integrated stimulator topology is approximately $\pm(V_{MAX} - V_D - V_{d,sat})$.

3.4.2   *Voltage Ripple*

For a given I_{STIM}, the "intrinsic" component of the observed DVS ripple depends on the DVS output voltage and the design choices used in implementing the switched-capacitor-based circuit (i.e. capacitor sizing, operating frequency, etc.). When placed in closed-loop feedback within a SUPPLY-configured PCD, as to supply I_{STIM} at a required average voltage level (described in Section 3.3.2), the voltage ripple amplitude can be further amplified, since the time between consecutive Φ pulses could be several f_{DVS} periods due to pulse-gating; when f_{DVS} pulses aren't forwarded through the pulse-gating circuit, the DVS is OFF and not supplying current, while I_{STIM} still loads the large output capacitor of the DVS, causing the DVS output voltage to decrease linearly versus time (a DVS is terminated, internally, by large output capacitor).

This same voltage ripple appears largely un-attenuated at both electrodes, and accordingly, also at the drain of the IDAC. Therefore, considering the worst-case ripple for a given I_{STIM}, the desired set voltage of the IDAC ($V_{d,sat}$ in Figure 3.4, Figure 3.5, and Figure 3.6 in Section 3.3) must be made sufficiently greater than the true dropout voltage of the IDAC so that the troughs of the ripple don't push the IDAC out of regulation. For a given I_{STIM}, the maximum ripple is observed at the minimum stimulation voltage; thus, for a given I_{STIM}, the required set voltage can

be determined by setting Z_E as a short and increasing the set voltage until the minimum observed IDAC voltage exceeds its true dropout voltage of the IDAC.

As I_{STIM} is decreased, lower input pulse signal (Φ) frequencies are required to run a loaded DVS (assuming a fixed design) across the 0V to V_{MAX} output range. Although pulse-gating can be used to generate a Φ with an average frequency less than f_{DVS}, if f_{DVS} is kept fixed the number of pulses forwarded by mistake, due to PCD loop delay, will have an increasingly amplified impact on the total ripple amplitude as I_{STIM} decreases. Accordingly, this ripple contribution can be kept more manageable as I_{STIM} is reduced by having the frequency generation block provide an f_{DVS} which, ideally, is just high enough in frequency to run the DVS, loaded by the reduced I_{STIM} level, up to V_{MAX}.

3.4.3   *PCD Loop Delay*

When placed in either the SUPPLY or TRACK configuration, the detected error of the PCD cannot be immediately quantized and applied to the pulse-gating circuit, and a forwarded Φ pulse cannot immediately produce a change in the DVS output voltage. Although the collective delay of the loop cannot lead to instability, it can increase the ripple voltage observed along the stimulus current path when a PCD is in the SUPPLY configuration, as well as introduce offset and negative overshoot during electrode tracking (i.e. when a PCD is in TRACK configuration); the implications of the former are discussed in Section 3.4.2, while the latter can lead to the high-side switch incidentally turning on and/or a large enough difference between DVS and electrode voltages being developed to result in the unreliable operation of the HVA that said DVS is biasing. Accordingly, in designing the comparators, pulse-gating circuit, and DVS, this collective PCD loop delay must be kept in mind.

3.4.4   *High-Voltage Circuits*

The DVSs, HVAs, and high-side switches are the only circuits that interface with potentially high-voltages during stimulus delivery. The high-voltage tolerance of these blocks is achieved through specialized circuit design (discussed in Chapter 4 and Chapter 5 for the DVS and HVA, respectively) and/or through the closed-loop operation of the PCDs, which keep each DVS output voltage approximately equal to the voltage of the electrode on the same side of the H-bridge (keeping the HVAs properly biased and the high-side switches reliably ON and OFF).

Accordingly, precautions must be made in assuring the DVS can adequately track a falling electrode voltage with worst-case |dV/dt| (determined by the maximum stimulus level and the parasitic capacitance which invariably appears at the electrode terminals due to HVA, high-side switch, pad, and off-chip contributions). Similarly, for a PCD in the SUPPLY configuration, the DVS (for a given f_{DVS} and I_{STIM}) must achieve a rise-time that does not take up a sizeable fraction of the total stimulus pulse-width. Accordingly, an HVA must be designed to reliably operate across the DVS output voltage and electrode voltage ranges, as well as across the range of DVS/electrode rise-times and fall-times (while considering worst-case offset between DVS and electrode voltages).

3.4.5 *Low-Voltage Circuits*

The high-voltage "specialized" DVS and HVA circuits (and the capacitive divider in the PCDs) allow standard circuit designs to be used in implementing the "low-voltage blocks" of the front-end. Although these blocks do not require specialized designs in terms of voltage tolerance, there are design considerations pertaining to other areas of performance that must be addressed by the implementation of each block.

3.4.5.1 Comparators

The proposed stimulator front-end requires the use of 3 to 4 comparators (3 if ε_{SUPPLY} generation and IDAC dropout detection are done by the same comparator). The ε_{SUPPLY} and ε_{TRACK} generating comparators must have sufficiently low delay (or must be clocked at a sufficiently high rate) to provide reliable PCD operation (i.e. not contribute exceedingly to the loop delay discussed in Section 3.4.3). The delay of dropout detecting comparator must also be sufficiently low, as to quickly force a transition to the next front-end configuration upon the event of IDAC dropout (before the IDAC goes much further towards/into dropout). The comparator used for ε_{SUPPLY} generation and/or dropout detection must have a common-mode input range the includes $V_{d,sat}$, which may be close to 0V.

Since the capacitive dividers of a PCD are reset to 0V, the common-mode input range of the ε_{TRACK} generating comparators must also include 0V. And because a ε_{TRACK} generating comparator is already detecting an attenuated difference signal, worst-case offset due to PVT must be considered when choosing its design. Also, since a ε_{TRACK} generating comparator is

measuring from the high-impedance output of a capacitive divider, the gate-leakage and kickback performance of its design must also be considered and evaluated while delivering a stimulus pulse of worst-case pulse-width.

3.4.5.2 IDAC

The IDAC should have sufficient output impedance to adequately regulate the stimulus current, during all phases of stimulus delivery, to approximately the same amplitude (which should be close to the nominal level). With that said, the operation of a PCD in the SUPPLY configuration (which keeps the IDAC voltage at a constant average level) and the presence of the HVAs (which limit the voltage seen by the IDAC as the electrode voltages increase to high levels) should relax said output impedance requirements to obtainable levels, without the use of very specialized/complex IDAC circuits.

To maximize the stimulator compliance, the IDAC should be implemented using a low-headroom design, with a $V_{d,sat}$ significantly closer to 0V than to VDD. Additionally, during stimulus delivery the drain voltage of the IDAC may increase very quickly, and the IDAC design must be able to handle such transient events without significant ringing/overshoot in the regulated current.

3.4.5.3 Low-Side Switch Sets

The low-side switch sets are used to pass voltages of different levels (with respect to an NMOS threshold voltage), and accordingly, Figure 3.2b (Section 3.2.1) shows the recommended implementation of each low-side switch within a given set. The SW_{GND} and SW_{IDAC} switches must be sized to handle the maximum level of expected stimulus; to control the time-constant of forced-discharge, it may be desired to make the ON-resistance of the SW_{GND} switches adjustable. If ε_{SUPPLY} generation and IDAC dropout detection are done by the same comparator, break-before-make (BBM) switching should be employed in driving the gates of the $SW_{CMP,0}$ and $SW_{CMP,1}$ devices.

3.4.5.4 Frequency Generation

On-chip "high-frequency" generation can be realized using a phase-locked loop (analog, digital, or mixed-signal implementation), with an RF signal or other source (e.g. a crystal) as the input reference. Since the pulse-width of a given stimulus waveform is likely significantly greater than

$1/f_{DVS}$ (or the sampling period of clocked comparators potentially employed by the PCDs), the requisite noise performance of the PLL is low, giving flexibility in other parameters of its design (e.g. power, bandwidth, form-factor).

Additionally, considering the PCD voltage ripple, for more uniform operation of the PCDs across the stimulus amplitude range, more than one frequency should be available for use as f_{DVS}. Such could be accomplished by making the output frequency of the PLL programmable, or by making divided-down versions of the PLL output frequency accessible. Since for most of the time the DVSs and PCDs will not be used to drive stimulus (i.e. the stimulator will be effectively off), the PLL should have a low-power mode of operation, and after being in such a mode, the PLL should be able to be reactivated without significant delay.

3.4.5.5 Digital Control

Non-event-triggered front-end configuration changes should be well synchronized to the system clock, and in a way that prevents glitches from manifesting during said configuration transitions. However, at the same time, the event of IDAC dropout detection should be able to force a configuration change, which is still synchronized across the front-end, but is not limited in speed by the frequency of the system clock, since the speed of this transition is desired to be quick, while the system clock frequency should be kept low to limit power consumption.

3.4.6 *Power Supplies*

In many standard CMOS processes, low-voltage devices and devices featuring thicker gate-oxide (e.g. "I/O" devices) are both available without extra processing steps. However, said devices would have different voltage ratings, with the later being elevated (i.e. LVDD vs. VDD). Accordingly, possible efficiency, form-factor, and compliance benefits may be gained by using an elevated supply and the more voltage-tolerant devices in implementing the DVSs and HVAs. If so, level shifters must be used to interface these blocks with their respective low-voltage, LVDD-powered, digital control modules. Additionally, the class of devices (i.e. VDD or LVDD) used to implement the low-side switches, the front-end of the IDAC, and the front-end of the ε_{SUPPLY} generating and dropout detecting comparator(s) depends on the voltage an HVA limits its low-side terminal to, which would likely be greater than LVDD (but less than VDD) if the thicker gate-oxide devices were to be used in its implementation.

Chapter 4. DYNAMIC VOLTAGE SUPPLY (DVS) CIRCUIT

This chapter covers the design, operation, and modeling of the dynamic voltage supply (DVS) circuit. First, an introduction is given in Section 4.1, covering the requisite functionality of the DVS circuit, and how previously developed circuits adequately, and inadequately, provide said functionality. Next, in Section 4.2, the transistor-level design of the DVS circuit is introduced, and its operation (including approximating expressions of power-conversion efficiency and output voltage) is discussed in the context of its two operational settings, which, collectively, provide the DVS functionality required by the stimulator front-end covered in Chapter 3. In Section 4.3, implementation considerations for the DVS circuit are discussed, including a recommended design methodology. Then, in Section 4.4, measurement results are provided for a stand-alone DVS fabricated in 65nm bulk-CMOS, which demonstrate the circuit functionality described in Section 4.2. Section 4.5 then concludes the chapter with a presentation of post-layout simulation results for the DVS implementation that is employed by the stimulator chip presented and discussed in Chapter 7.

4.1   INTRODUCTION

4.1.1   *Switched-Capacitor, Voltage-Boosting Circuits*

For the proposed CMOS stimulator front-end (covered in Chapter 3) to have high-voltage compliance, the dynamic voltage supplies (DVSs) of the system must be able to generate high-voltages using low-voltage bulk-CMOS devices. Charge-pump and voltage-doubler circuits have been previously developed, in a variety of bulk-CMOS-compatible topologies, to safely generate voltages, on-chip, exceeding VDD (i.e. the terminal-to-terminal voltage rating of the implementing transistors) [20-22]. Such circuits are typically inductorless (relying on switched-capacitor operation) and are based on a single-stage circuit, which can boost the output voltage with respect to the input by a voltage less than or equal to VDD; this single-stage circuit is then cascaded in-series to generate a "high" output voltage. Accordingly, the magnitude of the terminal-to-terminal voltages in each stage are kept within the foundry-defined device limits, while the voltage burden with respect to chip ground, which increases "going up" the multi-stage cascade, is placed on more voltage-tolerant structures like metal-insulator-metal (MiM)

capacitors and/or metal-oxide-metal (MoM) capacitors, as well as parasitic junctions in the process stack (e.g. the p-substrate-to-deep-n-well junction).

Applications involving these circuits (e.g. power management) may also require the output to be loaded with an average current draw. Therefore, while generating a high voltage such a circuit may also be required to move significant charge across a potential gradient. To estimate the performance under such loading conditions, the steady-state operation of charge pumps and voltage-doubler circuits can be approximated using the Thevenin model given in Equation 4.1, where I_L is the current being drawn by the load [20].

$$V_{OUT} = V_{OC} - I_L R_{INT} \tag{4.1}$$

The Thevenin, or "open-circuit" voltage (V_{OC}), of a multi-stage charge-pump/voltage-doubler circuit can be found by operating the circuit with only capacitive loading, and evaluating the output voltage after it has settled. The Thevinin resistance, or "internal resistance" (R_{INT}), models the ability of the switched-capacitor circuit to move charge from input to output while maintaining a potential gradient between input and output; in accordance with Equation 4.1, as the circuit is loaded by increased current, the output voltage decreases.

Considering this Thevinin model, many solutions may exist, even within the framework of a single charge pump/voltage-doubler circuit topology, to achieve a desired output voltage under a known loading condition. For example, to achieve 5V at the output with a 1mA load, a 10V V_{OC} circuit can be used with a 5kΩ R_{INT}, or likewise a 6V V_{OC} design with a 1kΩ R_{INT}; although in just considering the Equation 4.1 model the most power-efficient design of the two would be the former, the optimum V_{OC}, R_{INT} combination ultimately depends on other factors pertaining to the design and implementation of the underlying non-ideal circuit, such as power-conversion efficiency, form-factor, rise-time, voltage ripple amplitude, etc. Therefore, in designing an optimum DVS circuit, which must function as a power-supplying, voltage-boosting circuit within the proposed stimulator (see Chapter 3), the transient and power conversion efficiency performance must be extracted from the operation of the underling circuit, in addition to the R_{INT} and V_{OC}. However, the DVS circuit has unique performance requirements not typical for this class of circuits, in that it must be able to both supply and sink switched-capacitor current across a 0V to V_{MAX} output voltage range. Accordingly, a circuit must first be identified which meets said functional requirements. As it turns out, a suitable DVS circuit can be developed by

modifying the design of a voltage-doubler circuit; accordingly, as an introduction to this class of circuits, an overview of a voltage-doubler circuit is given next in Section 4.1.2.

4.1.2 *Voltage-Doubler Circuit Operation*

From a system-perspective, a DVS needs to foremost generate a variable voltage (0V to a maximum high voltage, V_{MAX}) while a constant current (i.e. the stimulus current) is drawn from the output. The voltage-doubler topology from [21] could potentially be configured to satisfy these power-supplying requirements while demonstrating relatively high efficiency at maximum output power (e.g. 50%); the schematic of this circuit is provided in Figure 4.1.
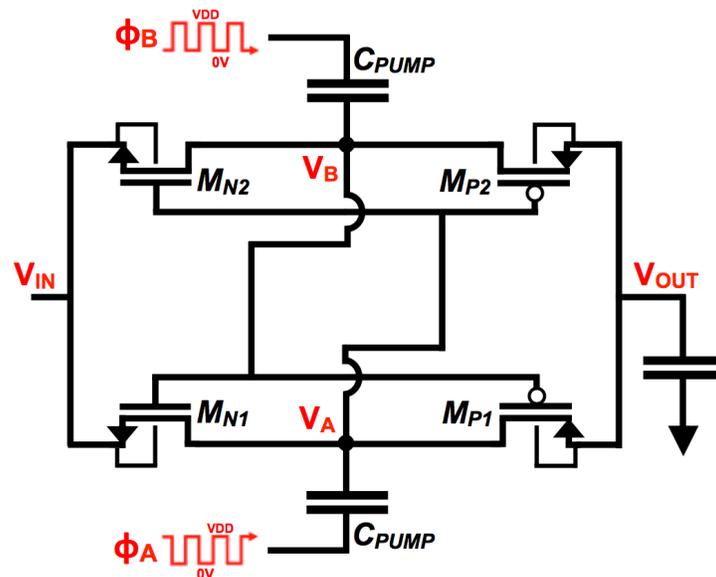
Figure 4.1. Voltage-doubler circuit, single-stage schematic [21]; Φ_A and Φ_B are complementary 50% duty-cycle pulse signals; $M_{N1,2}$ are DNW NMOS devices with DNW tied to V_{OUT}.

Unlike a classic Dickson charge-pump topology (discussed in [20]) the Figure 4.1 voltage-double circuit uses its PMOS and deep-n-well (DNW) NMOS devices as switches, as opposed to diode-connected-devices, to achieve increased voltage-boost per-stage. To prevent the degradation of switch functionality as the single-stage circuit is cascaded to achieve higher output voltage levels, the bodies of $M_{N1,2}$ and $M_{P1,2}$ are "locally" referenced to V_{IN} and V_{OUT}, respectively. Accordingly, with this topology the terminal-to-terminal voltages of $M_{N1,2}$ and $M_{P1,2}$ can be limited to be within $\pm$VDD (where VDD is the foundry-defined reliability limit of

the devices), all the while V_{IN} and V_{OUT} may be at voltages equal to several multiples of VDD. Therefore, the voltage burden is removed from individual transistors and instead placed on the C_{PUMP} capacitors (MoM, MiM, or stacked MOS-capacitor implementation); in a CMOS process the reverse-biased p-substrate-to-deep-n-well (PSUB/DNW) junction also carries this voltage burden. The Figure 4.1 circuit is also attractive for applications requiring high throughput current, fast rise-time, and minimum output voltage ripple due to the complementary switching of two conduction paths; i.e. with complementary pulse signals Φ_A and Φ_B of frequency f, the Figure 4.1 circuit delivers quanta of charge at a rate of 2f.

Although the operation of the Figure 4.1 circuit is well documented in [21], as well as in [20], it's worthwhile covering the basic operating principles of the circuit, as to understand its shortcomings for direct use as the DVS circuit.

4.1.2.1 Adequate DVS Power Supplying Functionality

To turn the top-plate switch devices on and off, the gates of M_{N1} and M_{P1} (M_{N2} and M_{P2}) in the Figure 4.1 single-stage circuit are driven by a DC level-shifted and high-pass filtered version of Φ_B (Φ_A). Assuming these devices, when applied these gate-driving signals, function as ideal switches with negligibly small ON-resistance (with respect to the period of Φ_A and Φ_B), the operation of the Figure 4.1 circuit (specifically, one of the conduction paths of said circuit) can be represented by Figure 4.2; as is apparent by Figure 4.2, this simplified model ignores any parasitic capacitances which may exist in the circuit.
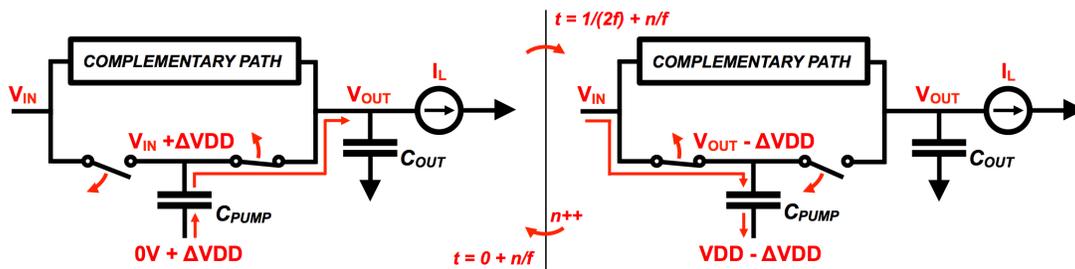
Figure 4.2. Simplified operational model of a single-stage voltage-doubler circuit at rising/falling pulse edges; $V_{IN} \leq V_{OUT}$.

Figure 4.2 shows that when the bottom-plate of C_{PUMP} is driven by a rising pulse edge at t = 0 + n/f, the same change in voltage appears at the top-plate of C_{PUMP}; at the same time the switches connecting the C_{PUMP} top-plate to V_{IN} and V_{OUT} open and close, respectively. After the

C_{PUMP} top-plate voltage is driven upwards (to a voltage greater than V_{OUT}), charge sharing between C_{PUMP} and C_{OUT} forces the C_{PUMP} top-plate voltage and V_{OUT} to equalize; the source of this charge-sharing current is the power-source attached to the bottom-plate of C_{PUMP} (i.e. VDD). Accordingly, the voltage stored across C_{PUMP} decreases during charge sharing, and this "lost" charge is either stored in C_{OUT} (boosting the output voltage) or is used to offset I_L.

A half-clock-cycle later the bottom-plate of C_{PUMP} is driven back down to 0V, while at the same time the switches connecting the C_{PUMP} top-plate to V_{IN} and V_{OUT} close and open, respectively. If charge sharing during the previous half-clock-cycle resulted in charge loss by C_{PUMP}, V_{IN} will recharge C_{PUMP} back up to $Q = C_{PUMP}V_{IN}$.

After enough time has passed, with the described operation repeating every 1/f interval, the circuit will reach a steady-state condition in which the output voltage is maintained at an average value that results in the average switched-capacitor current, supplied by the voltage-doubler, exactly offsetting I_L. Accordingly, at this steady-state condition, if $C_{OUT} \gg C_{PUMP}$, V_{OUT} can be treated as a DC voltage. Therefore, using the Figure 4.2 operational model the steady-state V_{OUT} can be approximated as a function of I_L, switching frequency f, C_{PUMP}, VDD, and V_{IN}.

Before and after charge sharing between C_{OUT} and C_{PUMP}, C_{PUMP} has a charge of $Q_0 = C_{PUMP}V_{IN}$ and $Q_1 = C_{PUMP}(V_{OUT} - VDD)$, respectively, as defined in Equation 4.2. Accordingly, Equation 4.3 gives the charge supplied by C_{PUMP} (to C_{OUT} and I_L) during said charge sharing.

$$Q_0 = C_{PUMP}V_{IN} , \quad Q_1 = C_{PUMP}(V_{OUT} - VDD) \tag{4.2}$$

$$Q_0 - Q_1 = C_{PUMP}(V_{IN} - V_{OUT} - VDD) \tag{4.3}$$

Considering both complementary switching paths, the Equation 4.4 equality can be derived by solving for the current corresponding to the packet of charge defined in Equation 4.3 delivered at a rate of 2f.

$$I_L = 2C_{PUMP}(V_{IN} - V_{OUT} + VDD)f) \tag{4.4}$$

Solving Equation 4.4 for the steady-state V_{OUT},

$$V_{OUT} = V_{IN} + VDD - I_L \left(\frac{1}{2fC_{PUMP}}\right) = V_{OC} - I_L R_{INT} \tag{4.5}$$

Equation 4.5 therefore gives the Thevinin equivalent approximation of the voltage-doubler circuit when operated under constant-current loading conditions; for resistive loading, $I_L =$

V_{OUT}/R_L must also be satisfied. The open-circuit voltage (V_{OC}) of the single-stage circuit is simply V_{IN} + VDD; accordingly if V_{IN} = VDD, the circuit can indeed "double" the input voltage if I_L = 0. The internal resistance term is inversely proportional to both the switching frequency f and the size of C_{PUMP}, and as such, for a given I_L, V_{OUT} can be made to approach V_{OC} by making f and/or C_{PUMP} larger.

Now consider a circuit consisting of "N" Figure 4.1 voltage-doubler circuits cascaded in-series. Keeping the same assumptions used in deriving Equations 4.2-4.5, and additionally assuming that the voltage at the output of each stage behaves like a DC signal at steady-state operation (a reasonable assumption considering the "differential" operation of adjacent stages which thereby places virtual grounds between stages), Equation 4.6 gives the Thevinin equivalent approximation of a multi-stage voltage-doubler circuit.

$$V_{OUT} = V_{IN} + N(VDD) - I_L \left(\frac{N}{2fC_{PUMP}} \right) = V_{OC} - I_L R_{INT} \qquad (4.6)$$

Considering Equation 4.6, a variable voltage generating circuit can be potentially designed using the Figure 4.1 topology, which, with a fixed C_{PUMP} and I_L, demonstrates a linear relationship between switching period (1/f) and V_{OUT}. Accordingly, 0V to V_{MAX} loaded operation (as required for adequate DVS functionality) can be achieved by setting V_{IN} to 0V, carefully choosing VDD, C_{PUMP}, and N to give a sufficiently high V_{OC} and a sufficiently low R_{INT}, and modulating the switching frequency f across a DC to f_{MAX} range, where at f = f_{MAX}, V_{OUT} = V_{MAX} (under worst-case loading conditions); and although Figure 4.2 and Equations 4.2-4.6 have been provided in the context of describing the operation of the Figure 4.1 circuit, this model can be readily used to approximate the operation of other voltage-doubler circuits with slightly different topologies (e.g. [22]), or charge-pumps, with comparable expressions for Dickson topologies given in [20].

Rise-time and voltage ripple are also important performance metrics. [21] demonstrates the fast rise-time (approximately 1μs) and small voltage ripple that can be afforded using the Figure 4.1 topology when the circuit is only clocked in the 100's of MHz, yet used to supply relatively high currents at voltages well exceeding VDD (i.e. 100's of μA, which are reasonable current levels for neural stimulation). Accordingly, from a power supply perspective, a voltage-doubler topology appears capable of providing the steady-state and transient performance required of a DVS for the proposed neural stimulation application.

4.1.2.2 Lack of Adequate DVS Discharge Functionality

Secondarily, but also critical to the operation of the stimulator, the DVS circuit must be able to actively discharge its output capacitor (which may be at any voltage in the 0V to V_{MAX} range) to a lower voltage in the same range, and such must be done in a controlled fashion which keeps the device terminal-to-terminal voltages within rated levels. With a purely capacitive load, the Figure 4.1 circuit, or the voltage-doubler circuits featured in [22], cannot provide this discharge functionality.

A resistive load (R_{OUT}) could be added in-parallel with C_{OUT} to allow the voltage across C_{OUT} to self-discharge. However, if this approach is used, there will be loss due to the presence of R_{OUT} when the circuit is operating as a power supply (i.e. the switched-capacitor current supplied by the circuit will have to offset both I_L and V_{OUT}/R_{OUT} to maintain a given V_{OUT} level). This problem is compounded by the fact that R_{OUT} will have to be made low enough to provide a sufficiently high C_{OUT} discharge rate (to track a falling electrode voltage when a PCD is in TRACK feedback, as discussed in Chapter 3).

There is a second issue in having the discharge of C_{OUT} be dependent on resistive loading. Considering a multi-stage circuit, the internal nodes between each stage (which could likely be higher than VDD) also need to be discharged as V_{OUT} decreases, and in a way that keeps the terminal-to-terminal voltages of the devices in each stage under the rated limits. Accordingly, during discharge, the Figure 4.1 circuit would still have to be operated in the same way as when supplying power, but the switching rate of the circuit would need to be low enough so that the switched-capacitor current supplied by the circuit is significantly less than V_{OUT}/R_{OUT} (else V_{OUT} will not decrease); operating the circuit like this would contribute to needless power consumption.

Lastly, considering the already discussed issues pertaining to resistive discharge, it would be exceedingly difficult to implement a reliable control scheme to force the output voltage of a multi-stage Figure 4.1 circuit to track a falling electrode voltage, and being able to control the DVS is this manner is critical to the operation of the overall stimulator front-end. Accordingly, modifications must be made to the Figure 4.1 voltage-doubler circuit in order to provide adequate discharge functionality, while leveraging and maintaining its adequate power-supplying functionality. Such a circuit has been realized, and is discussed in detail for the remainder of this chapter.

4.2   DVS CIRCUIT DESCRIPTION

To provide similar operation to the Figure 4.1 voltage-doubler circuit (discussed in Section 4.1.2) in terms of supplying (or "sourcing") switched-capacitor current, while also providing the discharging (or current "sinking") functionality that is required by the proposed stimulator front-end (see Chapter 3), a modified voltage-doubler circuit has been designed. The single-stage schematic of this DVS circuit is shown in Figure 4.3a, and a block diagram of the multi-stage configuration is shown in Figure 4.3b.
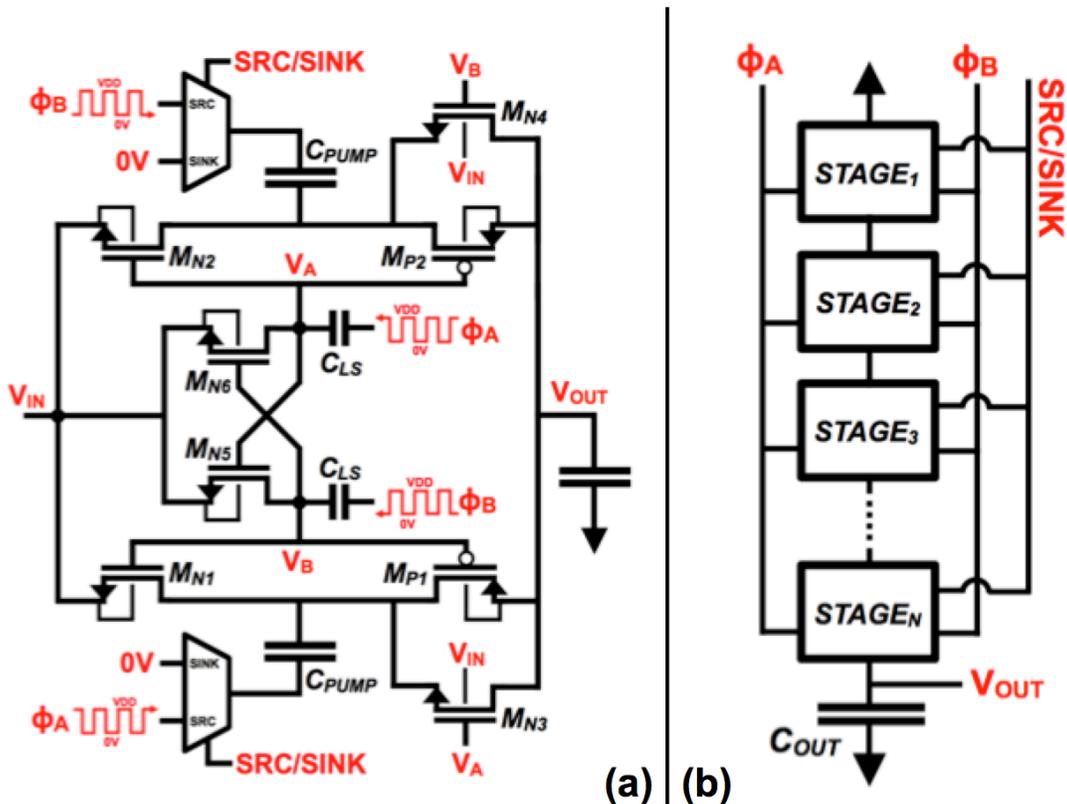
Figure 4.3. Proposed DVS circuit; (a) single-stage DVS circuit schematic ($V_{IN} \leq V_{OUT}$); (b) block diagram of multi-stage DVS circuit used in stimulator.

There are several notable differences between the Figure 4.3 DVS circuit and other voltage-doubler circuits [21, 22]. First, within the single-stage DVS circuit, 2-to-1 multiplexers are used to drive the bottom-plate of the C_{PUMP} capacitors, as opposed to directly driving these nodes with Φ_A and Φ_B, as is done in [21] and [22]. The deployment of these multiplexers allows the direction the DVS circuit moves switched-capacitor current to be chosen/changed: when in the

SOURCE setting (SRC used for brevity in Figure 4.3) the DVS sources, or supplies, switched-capacitor current to V_{OUT}; when in the SINK setting, the DVS sinks, or removes, switched-capacitor current from V_{OUT}. Accordingly, when the multiplexer control bit is set low (SOURCE is the active setting), these multiplexers feed through Φ_A and Φ_B (complementary 50% duty-cycle pulse signals) to the bottom-plates of C_{PUMP}, and as a result the DVS single-stage circuit functions as a voltage-boosting power-converter, with very similar functionality to the voltage-doubler circuits in [21] and [22]. When instead the multiplexer control bit is set high (SINK is the active setting), these multiplexers keep the bottom-plate of the C_{PUMP} capacitors at ground; this operation ultimately provides a multi-stage DVS with the current sinking functionality needed for the safe and controlled discharge of the output capacitance.

A second difference between the DVS and the other voltage-doubler circuits is how the top-plate switch devices are turned ON and OFF. In the Figure 4.3a single-stage circuit, the Φ_A and Φ_B pulse signals are transformed into $V_A = \Phi_A + V_{IN}$ and $V_B = \Phi_B + V_{IN}$, respectively, by a DC level shifter sub-circuit (composed of M_{N5}, M_{N6} and the C_{LS} capacitors); V_A and V_B are then applied to the gates of the top-plate switch devices ($M_{N1,2,3,4}$ and $M_{P1,2}$). In contrast, in the [21] voltage-doubler circuit covered in Section 4.1.2, the switch driving signals come directly from the top-plate of the C_{PUMP} capacitors; in a similar topology specialized for minimizing reverse leakage currents [22], the NMOS gate driving signals come from a DC level shifter sub-circuit while the PMOS gate driving signals come directly from the top-plate of the C_{PUMP} equivalent capacitors. Because all of the gate-driving signals of the DVS circuit are decoupled from the voltage at the top-plate of the C_{PUMP} capacitors, the DVS circuit can be operated in both its SOURCE and SINK settings, while other voltage-doubler topologies can only be operated in a SOURCE-equivalent setting.

The presence of the M_{N3} and M_{N4} devices (Figure 4.3a) is also unique to the proposed DVS circuit. When the DVS is in its SINK setting, these DNW NMOS devices allow V_{OUT} to be discharged completely to V_{IN} (if unloaded by a charge supplying source); if these device weren't present, V_{OUT} could not be reliably discharged below $V_{IN} + V_{th,p}$, where $V_{th,p}$ is the threshold voltage of the M_{P1} and M_{P2} devices.

Apart from these differences the proposed DVS circuit shares many similarities with previously developed voltage-doubler circuits. If loaded by constant-current I_L and configured to supply or "source" switched-capacitor current (i.e. SOURCE is the active DVS setting), the

steady-state operation of the single-stage DVS circuit can, like the [21] and [22] single-stage designs, be crudely approximated by the Figure 4.2 operational model and Equations 4.2-4.5 (presented in Section 4.1.2).

And like other voltage-doubler designs, N single-stage DVS circuits can be cascaded in-series to generate voltages exceeding VDD (Figure 4.3b), and Equation 4.6 in Section 4.1.2 can be applied to approximate the steady-state output voltage of the resulting multi-stage circuit. For a DVS employed by the proposed stimulator, V_{IN} must be set to ground to enable the required 0V to V_{MAX} output voltage range during SOURCE-setting operation and to allow V_{OUT} to be discharged down to 0V during SINK-setting operation. To prevent the body-effect from degrading the functionality of the switches as V_{IN} and V_{OUT} of a single-stage circuit increase (as these voltages would in an N-stage cascade), all NMOS devices shown in Figure 4.3a are implemented using deep-n-well (DNW) devices and the bodies of the NMOS and PMOS devices are tied to V_{IN} and V_{OUT}, respectively; likewise, the DNW of $M_{N1,2,3,4}$ are tied to V_{OUT} while the DNW of M_{N5} and M_{N6} are referenced to V_B and V_A, respectively. Accordingly, in a CMOS process the reverse breakdown voltage of the p-substrate-to-deep-n-well (PSUB/DNW) junction limits the maximum output voltage that can be generated by a DVS. The output of an N-stage DVS is connected to a large capacitor, C_{OUT}, where generally $C_{OUT} \gg C_{PUMP}$ as to reduce the amount of ripple observed at the DVS output. However, in sizing C_{OUT} there are rise-time/fall-time considerations, as well as form-factor limitation imposed by an integrated circuit implementation (no different than [21] and [22]).

Accordingly, the Figure 4.3 circuit can adequately satisfy the system-level DVS functionality demanded by the stimulator front-end proposed in Chapter 3. To demonstrate the relationship between relevant DVS performance metrics (e.g. power-conversion efficiency, maximum output voltage, rise/fall-time) and the elements of the Figure 4.3 circuit, Section 4.2.1 and Section 4.2.2 discuss the operation of the circuit in more detail within the context of each DVS settings (SOURCE and SINK, respectively).

4.2.1   *SOURCE-Setting Functionality*

The single-stage DVS circuit is configured as a charge sourcing (or charge supplying) circuit by setting the control bit to low (i.e. SOURCE). In this configuration, the complementary 50% duty-cycle pulse signals, Φ_A and Φ_B, are fed through by the bottom-plate multiplexers, while the DC level-shifted versions of the same signals (V_A and V_B) turn on and off the top-plate switch devices, as illustrated in Figure 4.4. The result is power-supplying operation that is functionally equivalent to the voltage-doubler circuits presented in [21] and [22].

Figure 4.4: Simplified DVS single-stage circuit for SOURCE-setting operation; $V_{IN} \leq V_{OUT}$.

With regards to operation within the stimulation front-end proposed in Chapter 3, when in the SOURCE setting an N-stage DVS is expected to be loaded by a constant current (i.e. the stimulus current), and accordingly, act as a charge-supplying power-converter with efficiency ε. Considering that a DVS my need to generate voltages much greater than VDD while supplying high stimulus currents (i.e. mA amplitudes), designing a DVS with maximum efficiency is important. Accordingly, modeling the loss mechanisms of the circuit and developing efficiency and output voltage estimates based on said modeling is a logical first step in realizing an optimal design.

Although Equations 4.2-4.5 from Section 4.1.2 can be applied to the DVS single-stage circuit to crudely approximate V_{OUT} based on C_{PUMP}, VDD, and the switching frequency, these

expressions ignore the parasitic capacitances that exist at the bottom-plate and top-plate of C_{PUMP}. Accordingly, the resulting model has no loss mechanisms, and cannot be used to estimate power-conversion efficiency. Additionally, these parasitics also affect the voltage-boost provided by each single-stage circuit, and therefore, considering a multi-stage DVS circuit, a large discrepancy may exist between a V_{OUT} estimation using Equation 4.6 (Section 4.1.2) and the simulated/measured value. Therefore, to get a rough estimate of DVS efficiency, as well as a more accurate estimation of V_{OUT}, an improved steady-state model that takes the parasitic capacitances of the circuit into account should be used; the derivation of such a model is given in Appendix B, with comparable models developed/used in [20] and [21].

This improved model makes the same assumptions as the simplified steady-state model used to derive Equations 4.2-4.6 (e.g. ideal switch behavior, V_{OUT} of each single-stage circuit behaving like a DC voltage at steady-state, etc.), but in this more representative model two parasitic capacitances are included: $C_{PAR,BP}$ and $C_{PAR,TP}$. $C_{PAR,TP}$ is the lumped parasitic capacitance appearing at the top-plate of each C_{PUMP}, and $C_{PAR,BP}$ is the lumped parasitic capacitance appearing at the bottom-plate of each C_{PUMP}. The main contributors to $C_{PAR,TP}$ are the C_{DG} capacitances of devices $M_{N1,2}$ and $M_{P1,2}$ and the C_{SG} capacitance of devices M_{N3} and M_{N4} (although since the gates of the latter two devices are driven in the same direction as the bottom-plate of the connected C_{PUMP}, their contribution to $C_{PAR,TP}$ is likely small compared to the other top-plate switch devices). Contributors to $C_{PAR,BP}$ include the intrinsic bottom-plate parasitic of the capacitor structure used to implement C_{PUMP}, as well as the capacitances associated with the digital buffer driving the bottom-plate (which may be quite large). Using the Appendix B model and considering an N-stage DVS with V_{IN} tied to ground, the following estimating expressions for V_{OUT}, P_{IN}, and ε can be derived.

$$P_{IN} = 2N\left(C_{PAR,BP} + \frac{C_{PAR,TP}C_{PUMP}}{C_{PUMP} + C_{PAR,TP}}\right)VDD^2 f + NI_L\left(\frac{C_{PUMP}}{C_{PUMP} + C_{PAR,TP}}\right)VDD \qquad (4.7)$$

$$V_{OUT} = N\left(\frac{C_{PUMP}}{C_{PUMP} + C_{PAR,TP}}\right)VDD - I_L\frac{N}{2f(C_{PUMP} + C_{PAR,TP})} = V_{OC} - I_L R_{INT} \qquad (4.8)$$

$$\varepsilon = \frac{V_{OUT}I_L}{P_{IN}} = \frac{\left(\frac{C_{PUMP}}{C_{PUMP} + C_{PAR,TP}}\right)I_L VDD - \frac{I_L^2}{2f(C_{PUMP} + C_{PAR,TP})}}{2\left(C_{PAR,BP} + \frac{C_{PAR,TP}C_{PUMP}}{C_{PUMP} + C_{PAR,TP}}\right)VDD^2 f + I_L\left(\frac{C_{PUMP}}{C_{PUMP} + C_{PAR,TP}}\right)VDD} \qquad (4.9)$$

Equation 4.9 shows that the estimated efficiency of a DVS (with the input tied to ground) is independent of N. However, Equation 4.8 shows that to supply I_L at a given output voltage level, a minimum N is required, and in increasing N from said minimum value, a larger R_{INT} term can be used (which can be changed independently of the V_{OC} by adjusting f, and/or changed by a much larger factor than the V_{OC} by adjusting C_{PUMP}, assuming $C_{PUMP} >> C_{PAR,TP}$).

Equations 4.7-4.9 also convey the efficiency-degrading mechanisms of the DVS circuit when in the SOURCE-setting. The P_{IN} expression shows there are CV^2f losses due to both $C_{PAR,BP}$ and $C_{PAR,TP}$, and the V_{OUT} expression shows that capacitive voltage division (via C_{PUMP} and $C_{PAR,TP}$) reduces the V_{OC} portion of the N-stage circuit's Thevenin model. Accordingly, attempts should be made to minimize these parasitics by not over-sizing the top-plate switch devices and bottom-plate driving buffers; however, in doing so said devices would no longer behave as "ideal" switches, and the measured/simulated performance of the resulting DVS would deviate from the Equation 4.7-4.9 estimations. Additionally, Equation 4.7 doesn't take into account the CV^2f losses associated with the parasitics of the C_{LS} capacitors (although such losses should be small compared to the Equation 4.7 P_{IN} estimation for a given DVS).

Rise-time and voltage ripple amplitude under I_L loading are also meaningful DVS metrics, and like other voltage-doubler circuits, both metrics depend on I_L, the frequency (f) of Φ_A and Φ_B, the size of C_{PUMP}, and the size of C_{OUT}. Qualitatively, and ignoring parasitics, the rise-time depends on how I_L compares to the current-driving ability of the DVS (the latter of which increases with increased f and/or C_{PUMP}), as well as the size of C_{OUT}. That is, for a given I_L, if the current-driving ability of a DVS is increased and/or C_{OUT} is decreased, the rise-time to a given voltage (under any definition) will decrease. Similarly, if the DVS parameters are fixed but the load current is increased, the observed rise-time to a given voltage will increase. Quantitative means of estimating rise-time, in the context of Dickson charge-pumps, can be found in [20]; an estimation method is also suggested in Section 4.3, in the context of the DVS functioning, with closed-loop regulation, within the proposed stimulator front-end.

Qualitatively, the voltage ripple amplitude is dependent on the output voltage of the DVS (with the largest ripple at low voltages), since the current-driving ability of the DVS is dependent on the output voltage. For a fixed output voltage, the observed ripple amplitude will increase if C_{OUT} is decreased. Additionally, in comparing two N-stage DVS designs, both loaded by I_L and exhibiting the same V_{OC} and R_{INT} (Equation 4.8) but implemented using a different Φ_A, Φ_B

frequency (f) and C_{PUMP} value, the design with the higher f (and lower C_{PUMP}) will have the smaller ripple amplitude, compared to the other, at every output voltage level. Equation 4.10, which is adapted from [20] and assumes steady-state DVS operation has been reached, provides a quantitative approach to conservatively estimate the DVS ripple amplitude.

$$V_R \approx {}^{I_L}\!/_{2fC_{OUT}} \qquad (4.10)$$

4.2.2 *SINK-Setting Functionality*

The single-stage DVS circuit is configured as a charge sinking circuit by setting the control bit to high (i.e. SINK). As shown in Figure 4.5, in this configuration the complementary 50% duty-cycle pulse signals, Φ_A and Φ_B, are only applied to the bottom-plates of the C_{LS} capacitors, while the bottom-plate of each C_{PUMP} capacitor is held at ground; the DC level-shifted versions of Φ_A and Φ_B (V_A and V_B) are then applied to the gates of the top-plate switch devices (to turn on and off), allowing charge to move from the output capacitance (initially charged to a voltage greater than V_{IN}) to C_{PUMP}, and subsequently from C_{PUMP} to V_{IN} (through each complementary conduction pathway).
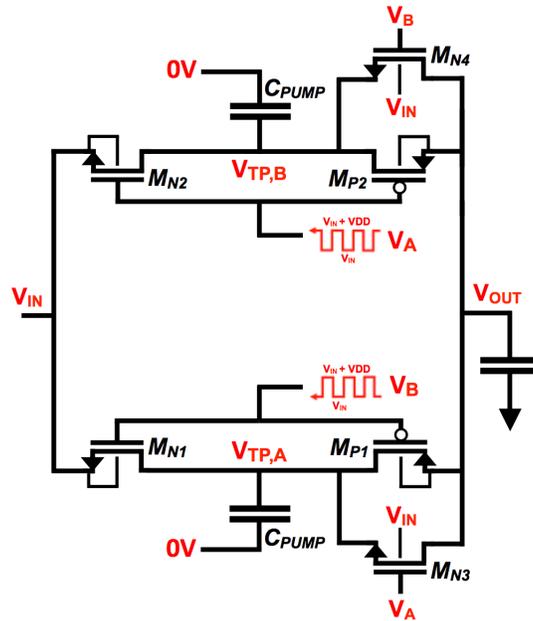
Figure 4.5. Simplified DVS single-stage circuit for SINK-setting operation; $V_{IN} \leq V_{OUT} \leq V_{IN} +$ VDD.

Section 4.2.1 and Appendix B employ an "improved" operational model of the DVS circuit to estimate the output voltage and power-conversion efficiency when the circuit is operating in the SOURCE setting and loaded by a sinking constant current, I_L. By using this same operational model (which takes into account the lumped parasitic capacitance at the top-pate and bottom-plate of each C_{PUMP}), but with I_L reversed in polarity (i.e. changed to a sourcing load) and the bottom-plate of each C_{PUMP} held at ground, one could derive Equation 4.11, which shows the Thevenin model of an N-stage DVS operating in the SINK setting.

$$V_{OUT} = I_L \frac{N}{2f(C_{PUMP} + C_{PAR,TP})} = V_{OC} + I_L R_{INT} \tag{4.11}$$

Accordingly, in comparing Equation 4.11 to Equation 4.8 (Section 4.2.1), the effective "internal resistance" (R_{INT}) of an N-stage DVS can be estimated using the same expression for both SOURCE and SINK operation models. Equation 4.11 also shows that if I_L is zero (i.e. the DVS is unloaded) then if given enough time the DVS output voltage can be discharged to 0V. Since charge is being brought from a high potential to ground, power-conversion efficiency really has no bearing for SINK-setting operation. However, operating the DVS in the SINK setting does require input power, namely the CV^2f power required to drive the bottom-plate and top-plate parasitics of the C_{LS} capacitors of the DC level shifter sub-circuit. However, the resulting input power should be small compared to the total P_{IN} observed during loaded SOURCE-setting operation.

Although Equation 4.11 provides a reasonable estimation of the steady-state output voltage of a DVS in the SINK setting, within the proposed stimulator the circuit is only used in this setting when unloaded, as to safely and controllably discharge the terminating C_{OUT} back to low-voltages. Accordingly, the fall-time performance of the DVS in this setting is important, and such can be estimated using the same means as suggested for SOURCE-setting operation in Section 4.2.1.

4.3   ADDITIONAL IMPLEMENTATION NOTES AND CONSIDERATIONS

4.3.1   *Operation within a PCD*

As described in Chapter 3, a SUPPLY-configured (TRACK-configured) positive-current driver controls the output voltage of a DVS operated in the SOURCE (SINK) setting via the generation of a 1-bit error signal, which is in turn used to gate individual pulse periods of a constant frequency clock, f_{DVS}, to create Φ; the complementary pulse signals Φ_A and Φ_B are then derived from Φ and used to drive the DVS. In a SUPPLY-configured positive-current driver (PCD) the stimulus current (with constant amplitude I_{STIM}) loads the DVS. Accordingly, considering the feedback employed by this PCD configuration, f_{DVS} pulse gating produces a Φ with an average frequency that sets V_{OUT}, on average, at the required level to keep the IDAC from dropping out, with V_{OUT} only expected to increase during this phase of stimulus delivery (i.e. the reactive component of electrode-tissue-interface impedance is expected to look capacitive). Therefore, during said operation Equations 4.7-4.9 in Section 4.2.1 can be utilized to relate the input power and the average frequency of Φ to the average output voltage of the DVS.

Estimating the transient operation of the DVS under such operating conditions may also be of interest, particularly the ΔV expected at the DVS output from each forwarded f_{DVS} pulse. For a given "DC" V_{OUT} level, a rough estimation of this ΔV can be derived by solving Equation 4.8 for I_L, where f is set to f_{DVS}, subtracting I_{STIM} from the resulting expression, and then solving for the voltage change that would be observed across the C_{OUT} of the DVS if the resulting difference current were applied to it over the duration of an f_{DVS} period. Knowing the worst-case ΔV for a given forwarded pulse could be useful in estimating the worst-case ripple amplitude at the DVS output due to ON/OFF regulation within a SUPPLY-configured PCD featuring loop-delay. Additionally, said ΔV expression could be applied to estimate the minimum rise-time from one DVS output voltage to another (through an iterative evaluation process).

Similarly, an expression estimating the $-\Delta V$ (due to a single forwarded pulse) at the unloaded DVS output when operating in a TRACK-configured PCD can also be derived for a given "DC" V_{OUT} level; i.e. by solving Equation 4.11 for I_L, where f is set to f_{DVS}, and then solving for the voltage change that would be observed across the C_{OUT} of the DVS if the resulting current were applied to it over the duration of an f_{DVS} period. Knowing the worst-case $-\Delta V$ for a given forwarded pulse is useful in assessing the negative over-shoot of the DVS in

tracking a falling electrode voltage (specifically when considering the delay of the TRACK-configured PCD loop). Additionally, said $-\Delta V$ expression could be applied to estimate the minimum fall-time from one DVS output voltage to another.

4.3.2 *Acceptable Rise/Fall-Time Performance*

For the proposed stimulator application, a DVS should be designed to reach its intended V_{MAX}, while loaded by the maximum stimulus current amplitude, within a time interval that is reasonably small compared to the minimum stimulation pulse-width (e.g. 10%). Since the DVS is unloaded during SINK operation, the minimum fall-time from V_{MAX} to ground should be significantly less than said rise-time. However, if the resulting fall-time performance is not sufficient for worst-case electrode voltage tracking, then parasitic capacitance can be intentionally placed at the electrode terminal to slow down the fall of the electrode voltage; the addition of said capacitance should not negligibly affect stimulator performance, as long the parasitic impedance is much greater than the expected impedance of the electrode-tissue-interface at frequencies relevant to stimulation.

4.3.3 *High-Frequency Gate-Oxide Voltage-Stress*

The proposed DVS circuit protects its transistors from low-frequency terminal-to-terminal voltages that exceed device voltage ratings. However, when in the SOURCE-setting the gate-to-drain voltage (V_{GD}) of several devices in a given single-stage circuit can momentarily exceed said voltage ratings, i.e. VDD, if the amplitude of the input-pulse signals (Φ_A and Φ_B) is set at (or close to) said VDD. This periodic instance of voltage stress occurs at the beginning of C_{PUMP} recharging, when the gate of M_{N1} (M_{N2}) in Figure 4.3 (Section 4.2) is forced high by V_B (V_A) while the bottom-plate of C_{PUMP} is brought down to 0V, resulting in a $-\Delta V$ at the drain of M_{N1} (M_{N2}).

With that said, depending on the switching frequency and the time-constant of charge-transfer, this periodic V_{GD} stress will likely be short lived within a given switching cycle, and is most problematic when the DVS output voltage is low; accordingly the low duty-cycle and high-frequency nature of said voltage stress should significantly reduce its effect on gate-oxide reliability over time. Furthermore, this periodic voltage stress is not unique to the DVS circuit, and can also occur within the [21] and [22] voltage-doubler circuits, which have been

demonstrated in silicon with the driving pulse signals having an amplitude set at the VDD-rating of the implementing devices.

However, if the described high-frequency voltage stress is a concern, the amplitude of Φ_A and Φ_B can be lowered, and/or the DC level shifter circuit can be designed to sufficiently capacitively divide Φ_A and Φ_B in generating V_A and V_B, respectively, via making C_{LS} sufficiently small and/or by making the top-plate parasitic of each C_{LS} intentionally larger.

4.3.4 *ESD Protection*

The DVS can be crudely protected from large positive voltages applied to the output (via an external source) by placing diode strings in-parallel with each stage. Accordingly, each diode string requires a turn-on voltage approximately equal to the VDD-rating of the devices used to implement the DVS, with the effective p-terminal (n-terminal) of each diode string connected to the output (input) of each DVS stage. P-implant-to-DNW or p-well-to-DNW diodes are suitable structures for this application, since such diodes can have the n-terminal be at high voltage (with respect to the substrate) only limited by the reverse breakdown voltage of the PSUB/DNW junction (just like the DVS output voltage). The forward turn-on voltage of the PSUB/DNW junction is used to crudely protect the DVS from the build-up of large negative voltages at the output.

4.3.5 *Design Methodology and Device Sizing*

The most critical performance metric of a DVS is its SOURCE-setting efficiency at maximum output power, since: 1) said maximum output power may be quite high (10's of mW) and the proposed stimulation system, if used in an implantable application, would have a strict power budget; 2) the current-driving ability required of a DVS (in the SOURCE setting) to meet the maximum output power requirement for many stimulation applications should provide for acceptable rise-time and fall-time performance; and 3) the proposed stimulation front-end design can withstand a fairly large ripple amplitude, and the ripple amplitude can always be reduced by making the C_{OUT} of a DVS larger.

Accordingly, C_{PUMP} (from Figure 4.3 in Section 4.2) should be sized to provide peak DVS efficiency when supplying maximum output power during SOURCE-setting operation (i.e. maximum stimulation current at V_{MAX}); Equations 4.7-4.9 in Section 4.2.1 can aide in this

optimization process, but to do so VDD, N, and the maximum Φ_A, Φ_B frequency (set by f_{DVS} in a PCD) must be known (or at least several values of each must be identified which could lead to practical/implementable DVS designs). However, in using Equations 4.7-4.9 the lumped top-plate and bottom-plate parasitic in each single-stage DVS circuit ($C_{PAR,TP}$ and $C_{PAR,BP}$, respectively) must be intelligently estimated.

The contribution from C_{PUMP} to $C_{PAR,BP}$, for a given capacitor structure in a given integrated process, should be able to be easily found via simulations, and should be proportional to the size of C_{PUMP}. The remaining contributions to each parasitic should be from the bottom-plate driving buffers and the top-plate switches. Accordingly, simulation tools and device models should be used to find scaling functions which relate the average ON-resistance (R_{ON}) of a bottom-plate buffer switch (NMOS or PMOS device of output inverter) and a top-plate switch (NMOS or NMOS device in-parallel with PMOS device), to the contribution each switch makes to $C_{PAR,TP}$ and $C_{PAR,BP}$ during SOURCE-setting operation. In finding said scaling functions, if the W of a device used to implement a switch increases by ΔW (L assumed fixed to minimum), then $1/R_{ON}$ and its parasitic contribution should also be expected to increase proportionally (approximately). In assuming every switch is sized to achieve a common R_{ON} resistance, R_{ON} can be estimated to be $1/(8\pi f_{DVS}C_{PUMP})$ and this estimated R_{ON} and the found $C_{PAR,TP}$ and $C_{PAR,BP}$ scaling functions can then be used to complete the estimate of the parasitics associated with a given DVS parameter set. With all parameters accounted for, Equations 4.7-4.9 can then be used to search for an optimum C_{PUMP} value.

After C_{PUMP} is determined, the scaling functions used to relate the R_{ON} of each DVS switch structure to its parasitic contribution can be utilized to size the transistors making up the top-plate switches and the output inverter of the bottom-plate buffers; depending on the size of said output inverter, a pre-driving inverter fan-out may be required. Likewise, the size of the devices implementing the top-side switches establishes the size of the C_{LS} capacitors (and accordingly the size of the buffers driving the bottom-plates of said capacitors) since the capacitance presented by the top-plate switch devices forms a capacitive divider with each C_{LS} capacitor, reducing the amplitude of the level-shifted versions of Φ_A and Φ_B. Therefore, there is a tradeoff between the amplitude of V_A and V_B (Figure 4.3, Section 4.2) relative to VDD, and the size of C_{LS} (and its pre-driving buffers). The DC level shifter devices, M_{N5} and M_{N6}, can be kept small since the recharging current required for each C_{LS} in a given switching cycle should be low.

However, Equations 4.7-4.9 do not consider the effects of switch resistance and non-complete charge transfer, and accordingly, with a DVS designed using the aforementioned process, a significant discrepancy may be observed between estimated and simulated performance. Therefore, after simulating an initial "optimized" design, the R_{ON} of the switches may need to be adjusted until desired performance is achieved. Such adjustment will likely require an iterative process, in which Equation 4.7-4.9 are reevaluated with updated scaling functions (taking into account an adjusted R_{ON}), as well as additional scaling functions that relate the size of R_{ON} to the size of C_{LS} and the size of the requisite pre-driver for the output inverter of a bottom-plate (C_{PUMP}) buffer, as to include the CV^2f losses associated with these supporting circuits into the input power and efficiency estimations.

Alternatively, if a model of a DVS can be developed which takes into account the R and C characteristics of the circuit, then a truly optimized DVS design could be potentially found, without using an iterative process of transistor-level simulations followed by design reevaluation, by employing said model, in conjunction with all of the described scaling functions. Such an R-C model is outlined in Appendix C.

4.4   FABRICATED DVS MEASUREMENTS

To demonstrate and verify the discussed functionality of the dynamic voltage supply (DVS) circuit, a 6-stage DVS has been fabricated in the TSMC 65nm GP CMOS process; a die photo of the test-chip is given in Figure 4.6, with the DVS highlighted. All of the NMOS and PMOS devices shown in the Figure 4.3 schematic (Section 4.2), as well as the bottom-plate driving buffers and multiplexers, are implemented using the 2.5V "I/O" devices of the process; to handle high load currents, these devices and bottom-plate buffers are sized for a maximum Φ_A, Φ_B frequency of 400MHz. C_{PUMP} and C_{OUT} are 2pF and 75pF, respectively, and are implemented using the metal-insulator-metal (MiM) capacitors available in the process. The PSUB/DNW reverse breakdown voltage, which sets the V_{MAX} of the fabricated DVS, is approximately 12V for the used process.
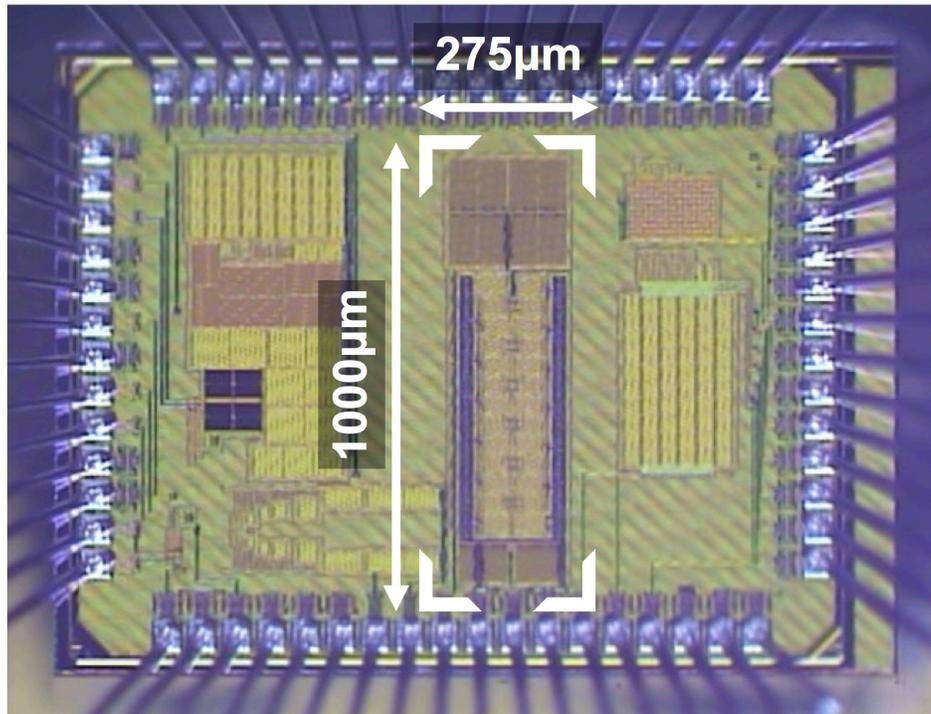
Figure 4.6. Stand-alone 6-stage DVS chip; fabricated in the TSMC 65nm GP CMOS process.

4.4.1 *Transient, Unloaded Performance*

Figure 4.7 shows the measured rise-time and fall-time of the described DVS, under non-loaded conditions and with the complementary input pulse signals (Φ_A, Φ_B) set to a constant frequency (120MHz). When configured like this, the DVS essentially operates like an inverting level shifter, transforming the SOURCE/SINK digital input into a 12V/0V digital output. Accordingly, even when operated at a relatively low switching rate (compared to the design's maximum rate of 400MHz) the fabricated DVS shows the ability to quickly traverse its 0V to 12V output range; the fall-time, specifically, demonstrates the ability of the DVS to track a falling electrode voltage if it were used in the stimulator front-end topology discussed in Chapter 3. Improved rise/fall-time performance with this design could be achieved by increasing the frequency of the input pulse signals; improved rise/fall-time performance with a different 6-stage DVS design, operated at the same frequency, could be achieved be increasing C_{PUMP} and/or decreasing C_{OUT}.
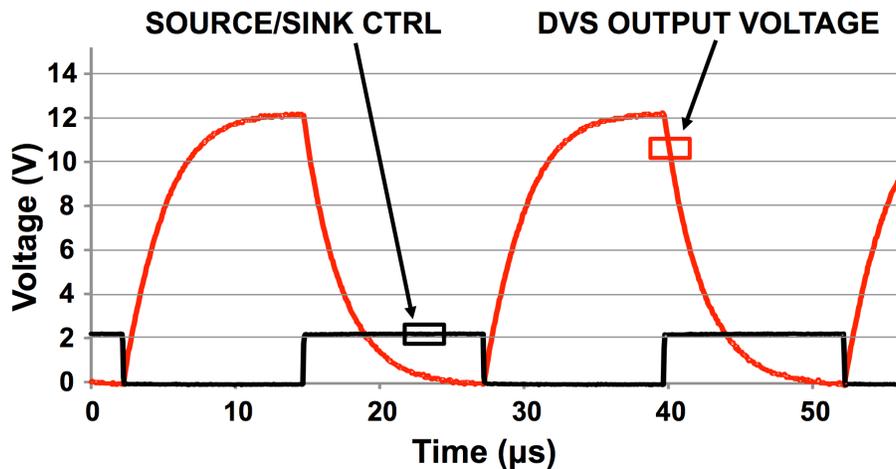
Figure 4.7. Measured unloaded DVS transient operation; 120MHz Φ_A and Φ_B, VDD = 2.3V.

4.4.2 *Steady-State, Loaded Performance*

A performance snapshot of the fabricated DVS under constant-current loading is provided in Figure 4.8, which shows the DVS output voltage versus input pulse signal (Φ_A, Φ_B) period, both measured and predicted, when the load current is set to 200μA. For both SOURCE and SINK settings, the predicted curve is generated using Equation 4.8 (Section 4.2.1) and Equation 4.11 (Section 4.2.2), respectively (with parasitics estimated from simulation results). Accordingly, for

both SOURCE and SINK settings, Figure 4.8 shows that the fabricated DVS behaves close to as predicted by said approximative expressions, and the larger difference in slope between the predicted/measured SOURCE curves (compared to the SINK curves) is attributed to reverse leakage current due to Φ_A, Φ_B overlap. These reverse leakage currents reduce power-conversion efficiency, and in future DVS iterations the magnitude of loss due to this mechanism can be easily reduced by using an improved non-overlapping clock generator.
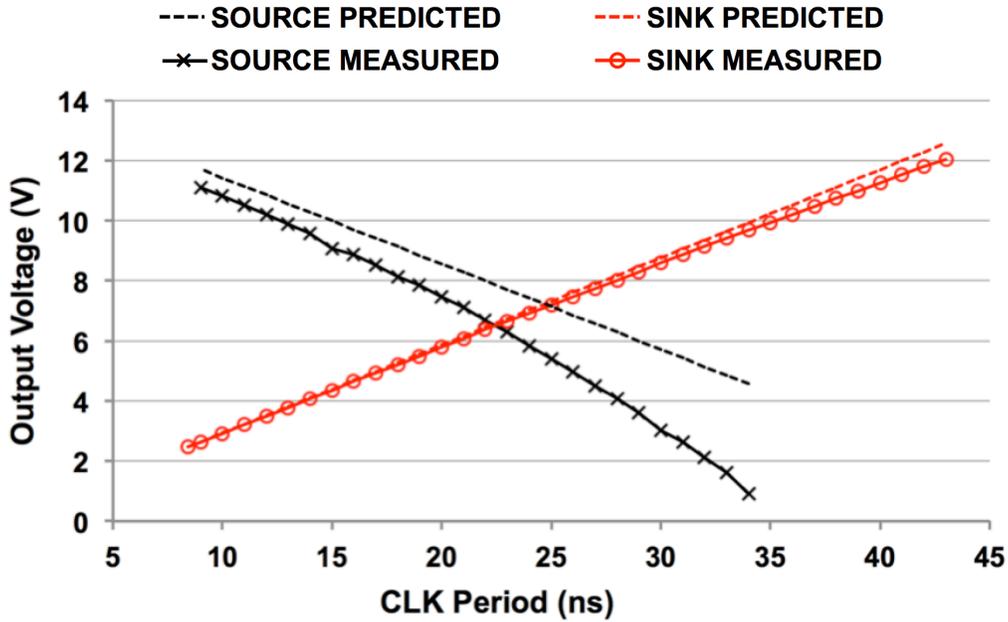
Figure 4.8. Measured steady-state DVS output voltage versus Φ_A and Φ_B period under 200µA constant-current load; VDD = 2.5V.

4.5 POST-LAYOUT SIMULATIONS

An 8-stage DVS has been designed in the TMSC 65nm GP CMOS process to deliver 2mA maximum current (in SOURCE setting) across a 0V to 12V output voltage range. The maximum expected frequency of Φ_A and Φ_B is 108.48MHz (i.e. the 13.56MHz ISM-band center frequency multiplied by 8). C_{PUMP} and C_{OUT} are set at 13.1pF and 180pF, respectively, and are implemented using the metal-insulator-metal (MiM) capacitors available in the process. To provide for maximum Φ_A and Φ_B amplitude (and therefore allow less DVS stages to be used in the design), 2.5V devices are used to implement the DVS transistors; accordingly, the DVS runs off of a nominal 2.5V VDD. The average ON-resistance of each top-plate switch is set at approximately 75Ω (when in the SOURCE-setting) and the average ON-resistance of the NMOS and PMOS devices which make up the output inverter of a bottom-plate buffer is approximately 55Ω; each bottom-plate buffer incorporates a 3-inverter fan-out to drive said output inverter. The C_{LS} capacitors of the DC level shifter sub-circuit (employed by each DVS stage) are set at 1.8pF.

These DVS design parameters were chosen using performance estimates provided by the R-C model outlined in Appendix C, in conjunction with the employment of parasitic estimating scaling functions (see Section 4.3.5), as to have the DVS display peak efficiency at maximum output power, and provide adequate power-supplying functionality if VDD were to drop from the nominal level by 5%. The total area of the described DVS is approximately 470mm^2, including over 140pF of decoupling capacitance (implemented using metal-oxide-metal, MiM, and MOS-capacitors).

Results from post-layout, extracted-view simulations of the described system, including a non-overlapping pulse generator (which creates Φ_A and Φ_B from Φ) operating off a nominal LVDD = 1V supply, as well as LVDD-to-VDD level shifters [25] for Φ_A, Φ_B and the SOURCE/SINK DVS control bit, are provided in Figure 4.9 and Figure 4.10.
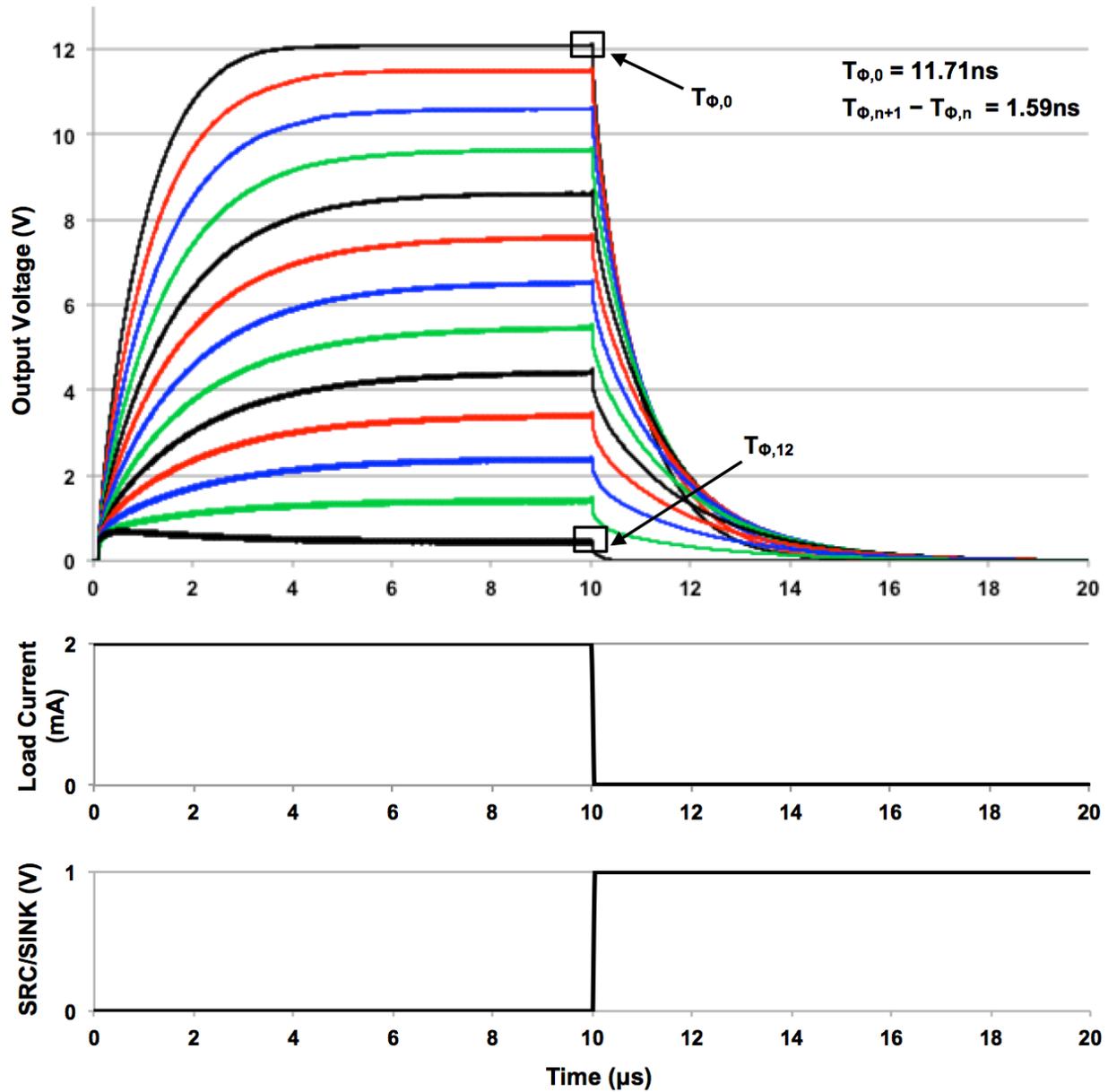
Figure 4.9. Transient, post-layout simulations of 8-stage DVS circuit (including non-overlapping pulse generation and level shifters) with varied period of input pulse signal, Φ; VDD = 2.5V, LVDD = 1V; in SOURCE setting, the DVS is loaded by 2mA constant-current; in SINK setting, the DVS is unloaded.
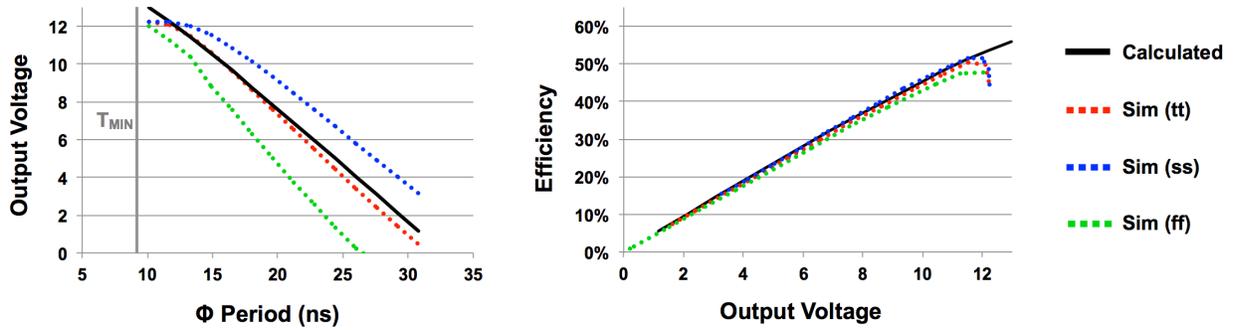
Figure 4.10. Steady-state, post-layout simulations (multiple corners) of DVS in SOURCE-setting with 2mA constant-current load and VDD = 2.5V, LVDD = 1V; on LEFT, output voltage versus Φ period (10.2ns to 30.79ns); on RIGHT DVS efficiency versus output voltage (observed when Φ varied from 10.2ns to 30.79ns); R-C model (Appendix C) and parasitic scaling functions used to "calculate" the predicted system performance.

Chapter 5. HIGH-VOLTAGE ADAPTER (HVA) CIRCUIT

In this chapter the operation and design of the high-voltage adapter (HVA) circuit, a critical functional block of the integrated stimulator front-end proposed in Chapter 3, is presented. An "ideal" HVA is first introduced in Section 5.1 and its operating principals are discussed, as to show how a low-voltage-device implemented circuit can provide the requisite high-voltage HVA functionality demanded by the proposed stimulator front-end. Then in Section 5.2, the transistor-level design of the actual HVA circuit is presented, which is an implementation of the ideal HVA that can be designed and fabricated in a real, low-voltage, bulk-CMOS process.

The design of the low-side switch set that interfaces with an HVA (within the stimulator front-end) is then discussed in Section 5.3, followed by Section 5.4, which summarizes the valid configurations of both an HVA and a low-side switch set, showing how each front-end block may be digitally reconfigured at different points during stimulus delivery. In Section 5.5 real-world implementation considerations pertaining to the design of both the HVA and a low-side switch set are discussed (e.g. device sizing, device voltage ratings, etc.), and the chapter is concluded with Section 5.6, which presents post-layout simulation results showing an HVA and low-side switch set functioning together under operating conditions that emulate what would be observed during stimulus delivery.

5.1 INTRODUCTION

From the perspective of the current stimulus, each HVA has two ports: a "high-side" port that is connected to an electrode and a "low-side" port that is connected to a set of low-voltage switches (which in turn can be configured to connect the low-side port to ground, the IDAC, and/or a comparator). The function of an HVA is therefore to provide an impedance pathway for current to flow between these two ports. In terms of operating within the proposed stimulator, such functionality requires: 1) an HVA to stay conductive across the entire electrode voltage range; 2) at low electrode voltages an HVA must exhibit low impedance, so that the effective resistance of the HVA doesn't produce a voltage which significantly reduces the stimulator compliance; and 3) at high electrode voltages an HVA must adequately limit the voltage at the low-side terminal to levels which are safe for the low-side circuits to interface with.

Accordingly an HVA requires the functionality of a high-voltage-tolerant NMOS device, which has its gate biased to V_{ON}, a voltage approximately equal to the voltage rating of the low-side circuits (i.e. VDD). At high electrode voltages, the drain-to-source voltage (V_{DS}) of such a device would absorb the voltage burden, while the source voltage, V_S (i.e. the voltage the low-side circuits see), would be limited to $V_{ON} - V_{GS}$, where V_{GS} is the gate-to-source voltage of this theoretical high-voltage-tolerant NMOS device; accordingly, V_S can be made to be less than or equal to VDD by setting V_{ON} to an appropriate voltage. At low electrode voltages, this high-voltage-tolerant NMOS device would behave in the triode region (if sized properly for the V_{ON} and stimulation currents used), and therefore exhibit a low drain-to-source resistance.

5.1.1 *Available Techniques to Achieve HVA-Like Functionality*

Circuits have been previously developed that demonstrate functionality similar to the requisite HVA functionality. In [23] a high-voltage digital buffer is presented. The buffer employs a PMOS device stack and an NMOS device stack (connected to a common output node), which are used to pass HVDD or 0V (or potentially another low voltage) to the output, respectively. The NMOS device stack is used like a high-voltage-tolerant NMOS switch (and the PMOS stack like a high-voltage-tolerant PMOS switch). When the NMOS stack is on and conducting, it is assumed that the PMOS stack is off (i.e. nonconductive) and the buffer output immediately drops to the low-voltage connected to the bottom-most source of the NMOS stack; accordingly, in this situation the gate-bias of each device in the NMOS stack is set to VDD. When the NMOS stack is off, it is assumed the PMOS device stack is passing HVDD to the buffer output, and the gates of the NMOS stack are biased to higher levels (i.e. to specific fractions HVDD) to assure V_{GS} and V_{DS} overstress do not occur in any of the NMOS devices.

However, there are issues with the [23] buffer topology in terms of adapting it for use as an HVA. First, the reliance on RC time-constants in setting the gate voltages of devices high up in each stack presents PVT sensitivity, and such sensitivity would only increase as more devices are added into each stack to realize a buffer that can interface with elevated HVDD levels. Secondly (and more problematically), the resistive dividers the buffer design relies on in dynamically changing gate voltages within the NMOS and PMOS stacks would need to be biased by a DVS (within the proposed stimulator design), with the DVS output voltage needing to be approximately equal to the buffer output for proper buffer functionality (like in [13, 14]). Under

such loading a DVS would no longer be able to track falling electrode voltages using ON/OFF regulation, which is a critical operating principle of the PCDs employed by the proposed stimulator.

In radio frequency (RF) and millimeter-wave (mm-Wave) transmitters, device stacking is sometimes used to implement the output stage of a power amplifier (PA), like the Class-E PA circuit presented in [24], as to enable larger signal swings at the PA output and boost the maximum transmit power. In [24] the NMOS device stack of the PA output stage has the top three devices DC-biased by low-pass networks (bottom device in the stack is driven by a pre-driver), with the DC voltage, passed to each gate, set to assure V_{DS} and V_{GS} overstress do not occur when the PA output is at its average voltage level. As the PA is used to drive an AC signal, the change in voltage from the average output level is distributed across the gates of the upper devices in the stack via a capacitive divider network, made up of the gate-to-drain capacitance (C_{GD}) and the gate-to-source capacitance (C_{GS}) of each stacked device, as well as the capacitors associated with the low-pass, DC-biasing networks. Accordingly, the capacitors in said network can be set, through careful device sizing, to provide a division ratio across the gates of the upper devices in the stack that prevents V_{GS} and V_{DS} overstress, throughout the device stack, as the PA output varies with maximum amplitude.

However, the several orders of magnitude difference between neural stimulation frequencies and RF frequencies (kHz versus GHz) presents implementation issues in terms of using the techniques demonstrated in [24] to realize a circuit with adequate HVA functionality. Specifically, the low-pass networks used to set the DC gate voltage of the upper devices in the stack would have to incorporate very large resistor and capacitor values (perhaps prohibitively large for silicon integration). The large capacitors of said low-pass filters would also affect the operation of the critical capacitive divider network, with the effective C_{GD} and C_{GS} capacitance of each device needing to be also boosted to larger values to prevent the low-pass filter capacitors from shunting-out the divider network.

With that said, if the resistors of each low-pass network could some how be set to infinity, after the "DC" value of each gate has been set, then some of the circuit techniques used in [24] could potentially be adapted for HVA use. Such describes the developed "ideal" N-stage HVA circuit, which is introduced next in Section 5.1.2.

5.1.2 *Ideal N-Stage HVA Circuit*

Although high-voltage-tolerant NMOS devices aren't typically available in standard, low-voltage CMOS processes, a circuit with the same functionality can be created using a stack of N identical deep-n-well (DNW) NMOS devices (with source-body, drain-DNW tying), as shown in Figure 5.1. The Figure 5.1 circuit is defined as an "ideal" N-stage HVA.
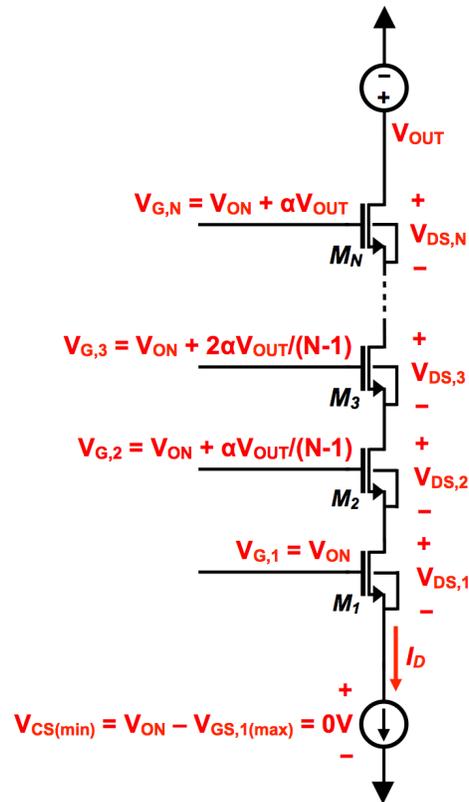
Figure 5.1. An ideal N-stage HVA for $V_{OUT} \geq 0$; gate-biasing function assures device terminal-to-terminal voltages stay below the device voltage rating (VDD) if V_{ON}, N and α are properly set for maximum expected output voltage; M_1 through M_N have same W and L.

If across the expected output voltage range the V_{GS} and V_{DS} of all the HVA devices can be assured to be less than or equal to the foundry-defined voltage rating of the implementing transistors (i.e. VDD), then all device terminal-to-terminal voltages should always be at safe levels, and the reliability of the HVA structure over time should not be compromised due to voltage overstress. Such reliability assurance can be achieved if the gate-biasing function,

provided in Equation 5.1 and illustrated in Figure 5.1 for $V_{OUT} \geq 0$, has its parameters carefully set.

$$V_{G,k} = V_{ON} + \alpha \left(\frac{k-1}{N-1}\right) V_{OUT}, \quad \text{where} \quad V_{ON} < VDD, \ V_{OUT} \geq 0 \tag{5.1}$$

For $V_{OUT} \geq 0$, the gate-biasing function has two components: a DC offset (V_{ON}) and an amplified version of V_{OUT}. V_{ON} is chosen to make the collective V_{DS} of the HVA stack small at low electrode voltages, so that when functioning within the stimulus current path of a SUPPY-configured positive-current driver (PCD), the HVA doesn't significantly reduce the stimulator compliance at maximum stimulus current levels (i.e. at maximum drain current, I_D, levels in Figure 5.1). V_{ON} also has to be set keeping the V_{GS} reliability of the top-most device (M_N) in mind, as is further discussed in Section 5.1.4. The "gain" of the amplified V_{OUT} term in Equation 5.1 has two coefficients: 1) a constant coefficient (α) which is independent of k and N, and 2) a k-dependent (and N-dependent) term which is 1 when k = N, and decreases by constant increment moving down the device stack, until it equals 0 for k = 1.

The constant coefficient α is set to satisfy Equation 5.2 (where $V_{OUT(max)}$ is the maximum output voltage the HVA can interface with) and the k-dependent coefficient provides for the Equation 5.3 equality. Accordingly, the Equation 5.1 gate-biasing function, with α set properly, makes Equation 5.4 true across the positive V_{OUT} range of the circuit, and makes Equation 5.5 true when $V_{OUT} = V_{OUT(max)}$.

$$V_{G,N} - V_{G,1} = (N-1)VDD = \alpha V_{OUT(max)} \tag{5.2}$$

$$V_{G,k} - V_{G,k-1} = \alpha \frac{V_{OUT}}{N-1} \quad \text{for} \quad k = 2, \dots, N, \ 0 \leq V_{OUT} \leq V_{OUT(max)} \tag{5.3}$$

$$0 \leq V_{G,k} - V_{G,k-1} \leq VDD \quad \text{for} \quad k = 2, \dots, N, \ 0 \leq V_{OUT} \leq V_{OUT(max)} \tag{5.4}$$

$$\left[V_{G,k} - V_{G,k-1}\right]_{@V_{OUT(max)}} = VDD \quad \text{for} \quad k = 2, \dots, N \tag{5.5}$$

Considering Equations 5.2-5.5 it can be shown that if α falls above a lower limit, then the V_{DS} reliability of each device in the HVA device stack can be assured. Additionally, if V_{ON} is set sufficiently below VDD, it can be shown that an upper limit of α also exists, which if α falls below V_{GS} reliability throughout the device stack can be assured. However, the validity of both limits is based on the assumption that V_{OUT} stays below its maximum value, which from

Equation 5.2 can be defined as Equation 5.6. Therefore, a range of "safe" values of α can exist, as shown by Equation 5.7, where Equation 5.8 and Equation 5.9 define α_{min} and α_{max}, respectively. Section 5.1.3 and Section 5.1.4 of this chapter provide the derivations of these two limits (α_{min} and α_{max}, respectively) in detail.

$$V_{OUT(max)} = (N-1)VDD/\alpha \tag{5.6}$$

$$V_{DS,k} \leq VDD, \ V_{GS,k} \leq VDD \quad \text{if} \quad \alpha_{min} \leq \alpha < \alpha_{max}, \ 0 \leq V_{OUT} \leq V_{OUT(max)} \tag{5.7}$$

$$\alpha_{min} = (N-1)/N \tag{5.8}$$

$$\alpha_{max} = \frac{(N-1)VDD}{V_{ON} + (N-2)VDD} \tag{5.9}$$

5.1.3 *Drain-to-Source Reliability*

Considering Equations 5.2 and 5.3, the V_{DS} of each device in an ideal, N-stage HVA (Figure 5.1) can be determined using Equation 5.10. Accordingly, the functions governing the V_{DS} of device M_k (up to k = N − 1) and the V_{DS} of device M_N have different forms, and conditions must be found which insure $V_{DS,k} \leq VDD$, for both sets of device indices.

$$
\begin{aligned}
V_{DS,k} &= \begin{cases} \left(V_{G,k+1} - V_{GS,k+1}\right) - \left(V_{G,k} - V_{GS,k}\right) & \text{for } k = 1, \dots, N-1 \\ V_{OUT} - \left(V_{G,k} - V_{GS,k}\right) & \text{for } k = N \end{cases} \\
&= \begin{cases} \alpha\frac{V_{OUT}}{N-1} + V_{GS,k} - V_{GS,k+1} & \text{for } k = 1, \dots, N-1 \\ (1-\alpha)V_{OUT} - V_{ON} + V_{GS,k} & \text{for } k = N \end{cases}
\end{aligned} \tag{5.10}
$$

Equations 5.4 and 5.5 show that the difference voltage between adjacent gates in an HVA stack has a maximum of VDD, which should occur when $V_{OUT} = V_{OUT(max)}$. Accordingly, considering Equations 5.3-5.5, and 5.10, the following inequality can be defined,

$$V_{DS,k} \leq VDD + V_{GS,k} - V_{GS,k+1} \quad \text{for } k = 1, \dots, N-1 \tag{5.11}$$

To satisfy Equation 5.11, $V_{GS,k} - V_{GS,k+1}$ must be forced to be less than or equal to zero. Since every device in an HVA stack is identical and has the same drain current (I_D), this condition can be assured if, going up the device stack, from M_1 to M_N, devices only move more towards (or within) the triode region of operation; that is,

$$V_{DS,k} \leq VDD \quad \text{if} \quad V_{DG,k} \geq V_{DG,k+1} \qquad \text{for } k = 1, \dots, N-1 \tag{5.12}$$

By the same condition, V_{DS} reliability for M_N can be assured; that is,

$$V_{DS,N} \leq V_{DS,N-1} \leq VDD \quad \text{if} \quad V_{DG,N-1} \geq V_{DG,N} \tag{5.13}$$

Equations 5.14 and 5.15 define the drain-to-gate voltage (V_{DG}) of M_k (up to k = N − 1) and M_N, respectively.

$$V_{DG,k} = V_{G,k+1} - V_{GS,k+1} - V_{G,k} = \alpha \frac{V_{OUT}}{N-1} - V_{GS,k+1} \quad \text{for } k = 1, \dots, N-1 \tag{5.14}$$

$$V_{DG,N} = V_{OUT} - V_{G,N} = (1-\alpha)V_{OUT} - V_{ON} \tag{5.15}$$

Assuming the HVA has at least 3 stages (i.e. N ≥ 3), Equation 5.14 can be used to derive Equation 5.16, which defines $V_{DG,2}$ and $V_{DG,1}$ in terms of $V_{GS,3}$ and $V_{GS,2}$.

$$V_{DG,2} - V_{DG,1} = V_{GS,2} - V_{GS,3} \tag{5.16}$$

The right side of Equation 5.16 will be negative if $V_{DG,3} < V_{DG,2}$ (i.e. $V_{GS,3} > V_{GS,2}$), and if such is the case, to satisfy the equality, $V_{DG,1}$ will be forced to be greater than $V_{DG,2}$. Accordingly, this relationship between $V_{DG,k}$, $V_{DG,k+1}$, and $V_{DG,k+2}$ can be extended up the HVA stack (see Equation 5.17). Furthermore, Equation 5.16 can also be used to deduce Equations 5.18 and 5.19. Therefore, if $V_{DG,N}$ can be assured to be less than or equal to $V_{DG,N-1}$, then both Equations 5.12 and 5.13 will be true (for any N) and V_{DS} reliability for all of the HVA devices can be guaranteed.

$$V_{DG,k} > V_{DG,k+1} \quad \text{if} \quad V_{DG,k+1} > V_{DG,k+2} \qquad \text{for} \quad k = 1, \dots, N-2 \tag{5.17}$$

$$V_{DG,k} = V_{DG,k+1} \quad \text{if} \quad V_{DG,k+1} = V_{DG,k+2} \qquad \text{for} \quad k = 1, \dots, N-2 \tag{5.18}$$

$$V_{DG,k} < V_{DG,k+1} \quad \text{if} \quad V_{DG,k+1} < V_{DG,k+2} \qquad \text{for} \quad k = 1, \dots, N-2 \tag{5.19}$$

Equations 5.20 and 5.21 provide the derivation of α_{th}, the value of α which provides for the $V_{DG,N} = V_{DG,N-1}$ condition.

$$V_{DG,N} = V_{DG,N-1} \quad \text{if} \quad (1-\alpha_{th})V_{OUT} - V_{ON} \leq \alpha_{th}\left(\frac{1}{N-1}\right)V_{OUT} - V_{GS,N} \tag{5.20}$$

$$\alpha_{th} = \left(\frac{N-1}{N}\right)\left(1 + \frac{V_{GS,N} - V_{ON}}{V_{OUT}}\right) \tag{5.21}$$

α_{th} marks an important threshold. If $\alpha = \alpha_{th}$, then all devices in the stack will have the same V_{GS} (see Equation 5.18). If $\alpha > \alpha_{th}$, then in moving down the HVA stack the V_{GS} of devices will decrease (see Equation 5.17). If $\alpha < \alpha_{th}$, then in moving down the stack the V_{GS} of devices will increase (see Equation 5.19). Accordingly, to satisfy V_{DS} reliability, α must be greater than or equal to α_{th}.

Since $\alpha = \alpha_{th}$ sets all devices in the stack to have the same V_{GS}, V_{DG}, and V_{DS}, then $V_{GS,N}$ in Equation 5.21 can be substituted with $V_{GS,1}$, where $V_{GS,1} \leq V_{ON}$. Accordingly, Equation 5.21 can be evaluated at the maximum expected $V_{GS,1}$ (i.e. $V_{GS,1}$ at the maximum expected I_D) and the maximum expected V_{OUT} to give $\alpha_{th(max)}$ (Equation 5.22), which, for a given N, is the highest possible α_{th} value. Accordingly, if $\alpha \geq \alpha_{th(max)}$, then $\alpha \geq \alpha_{th}$ for any possible set of V_{OUT} and I_D operating conditions the HVA may see.

$$\alpha_{th(max)} = \left(\frac{N-1}{N}\right)\left(1 + \frac{V_{GS,1(max)} - V_{ON}}{V_{OUT(max)}}\right) \tag{5.22}$$

To give the most conservative evaluation of $\alpha_{th(max)}$, $V_{GS,1(max)}$ can be assumed to be V_{ON}, giving Equation 5.23, which can be applied as the lower bound of α to assure V_{DS} reliability throughout the HVA device stack.

$$\alpha_{min} = (N-1)/N \tag{5.23}$$

Accordingly, Equations 5.12 and 5.13 can be rewritten and combined as Equation 5.24, in which the Equation 5.6 definition of $V_{OUT(max)}$ is used.

$$V_{DS,k} \leq VDD \quad \text{if} \quad \alpha_{min} \leq \alpha, \quad 0 \leq V_{OUT} \leq V_{OUT(max)} = (N-1)VDD/\alpha \tag{5.24}$$

5.1.4 Gate-to-Source Reliability

Section 5.1.3 shows that if the constant gain term (α) of the Equation 5.1 gate-biasing function falls above a minimum value, α_{min}, then V_{DS} reliability can be assured throughout the HVA device stack, and the V_{GS} of device M_k will be less than or equal to the V_{GS} of device M_{k+1}. Therefore, assuming $\alpha \geq \alpha_{min}$, if a condition can be found which protects the top-most HVA device (M_N) from V_{GS} levels exceeding VDD, than V_{GS} reliability throughout the entire HVA stack can also be assured.

Such a condition can be easily established if one assumption is made: as the gate-to-drain voltage (V_{GD}) of device M_N approaches its maximum allowed value (i.e. approaches VDD), its resulting V_{DS} will be very small (compared to VDD). Such an assumption would therefore make Equation 5.25 reasonably true.

$$V_{GS,N(max)} \approx V_{GD,N(max)} < VDD \tag{5.25}$$

Maximum $V_{GD,N}$ will occur for a given value of α when $V_{G,N}$ and V_{OUT} are at their respective maximum values.

$$VDD > V_{GD,N(max)} = [V_{ON} + VDD(N - 1)] - V_{OUT(max)} \tag{5.26}$$

Solving for $V_{OUT(max)}$,

$$V_{OUT(max)} > [V_{ON} + VDD(N - 2)] \tag{5.27}$$

Substituting in Equation 5.6 for $V_{OUT(max)}$ in Equation 5.27 and solving for α gives the limit of α_{max}, which, if α falls below, V_{GS} reliability throughout the entire HVA should be reasonably assured.

$$\alpha < \alpha_{max} = \frac{(N - 1)VDD}{V_{ON} + VDD(N - 2)} \tag{5.28}$$

However, for α_{max} to be reliable in terms of assuring the HVA devices aren't overstressed, Equation 5.25 must hold at the maximum drain current (I_D) level, which will occur for a given N, α, and V_{OUT} when device M_1 has a V_{GS} of V_{ON}. Accordingly, it's possible the Equation 5.25 assumption will not hold up if V_{ON} isn't sufficiently lower than VDD; i.e. when $V_{GD,N}$ = VDD, the resulting $V_{DS,N}$ may be non-negligible, potentially forcing $V_{GS,N}$ to device-damaging levels. Accordingly, to prevent possible V_{GS} overstress in device M_N at the maximum I_D setting, V_{ON} can be lowered until Equation 5.25 is reasonably true. Alternatively, α can be set sufficiently lower than α_{max} so that $V_{GD,N(max)}$ will fall significantly below VDD at the maximum I_D level. Both of these two adjustments require the use of simulation tools. Accordingly, α_{max} can be thought of as an initial upper bound, which can be manually evaluated and lowered as needed by the designer based on the parameters of a specific HVA implementation (e.g. device models, V_{ON}, etc.).

5.1.5 *Negative Output Voltage Reliability*

During stimulus delivery the output voltage of an HVA can go negative (with respect to chip ground). This situation only occurs at the beginning of balancing-pulse delivery, when ground is used at the low-impedance node of the H-bridge front-end and the electrode-tissue-interface impedance is discharged by the stimulus current. Accordingly, the negative voltage at V_{OUT} is the result of the stimulus current going through the collective drain-to-source resistance of the device stack. Figure 5.2 illustrates this situation occurring with an ideal N-stage HVA; the new gate-biasing scheme shown is only valid for $V_{OUT} < 0$.
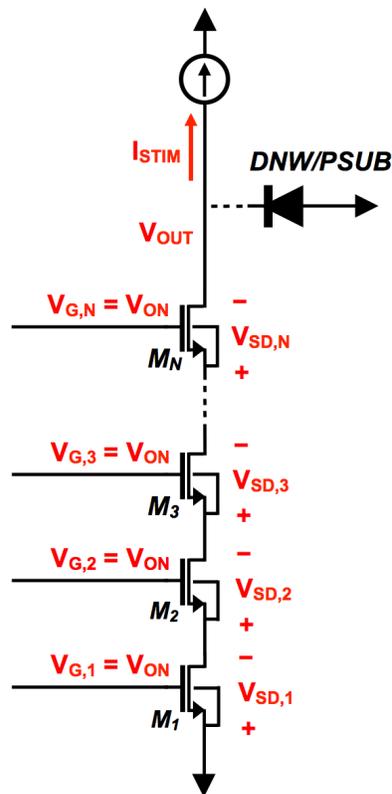
Figure 5.2. An ideal N-stage HVA for $V_{OUT} < 0$; every gate voltage equals V_{ON}; source/drain labeling used to maintain consistency with Figure 5.1; "functional" source of each device is labeled drain, and vice-versa.

For $V_{OUT} \geq 0$, a minimum V_{OUT} is required to keep the current source, regulating I_D (i.e. the stimulus current), from dropping out. Accordingly, to minimize this voltage, the HVA devices should be sized to have a collectively small drain-to-source resistance at low V_{OUT} levels, so that

the resulting voltage drop across the HVA at the maximum stimulus level is significantly less than VDD.

Accordingly, when $V_{OUT} < 0$ and current is going in the opposite direction through the HVA stack, the collective drain-to-source resistance of the stack should be even lower, since the functional V_{GS} of each device will be larger and the body of each device will be at a higher voltage than its functional source, reducing the threshold of each device compared to the threshold observed during $V_{OUT} \geq 0$ operation. Therefore, the low resistance of the HVA should alone be sufficient in protecting its devices from both V_{DS} and V_{GS} overstress, but as a further fail safe, the p-substrate-to-deep-n-well (PSUB/DNW) junction, with the n-terminal seen by V_{OUT} due to DNW-drain tying, will begin conducting at an output voltage likely higher than $-(VDD - V_{ON})$, which is the minimum allowed output voltage for the ideal HVA circuit (assures V_{GS} and V_{DS} reliability for M_N, and accordingly, and for all other devices in the HVA stack).

Considering this gate-biasing scheme, the Equation 5.1 gate-biasing function can be updated to be valid across the entire valid range of V_{OUT} (see Equation 5.29).

$$V_{G,k} = V_{ON} + max\left\{0, \ \alpha\left(\frac{k-1}{N-1}\right)V_{OUT}\right\}$$

$$\text{where} \quad V_{ON} < VDD, \ -(VDD - V_{ON}) \leq V_{OUT} \leq V_{OUT(max)} \tag{5.29}$$

5.2   HVA CIRCUIT DESCRIPTION

Figure 5.3 provides the schematic of the HVA circuit employed by the proposed integrated stimulator front-end, which is a realization of the "ideal" HVA circuit (discussed in Sections 5.1.2-5.1.5) that can be implemented in a low-voltage, bulk-CMOS process. The number of "stages" in the Figure 5.3 N-stage circuit is set according to the voltage rating of the devices used to implement each stage (i.e. VDD) and the maximum voltage the HVA is expected to interface with (i.e. $V_{OUT(max)}$), just like the ideal HVA circuit.
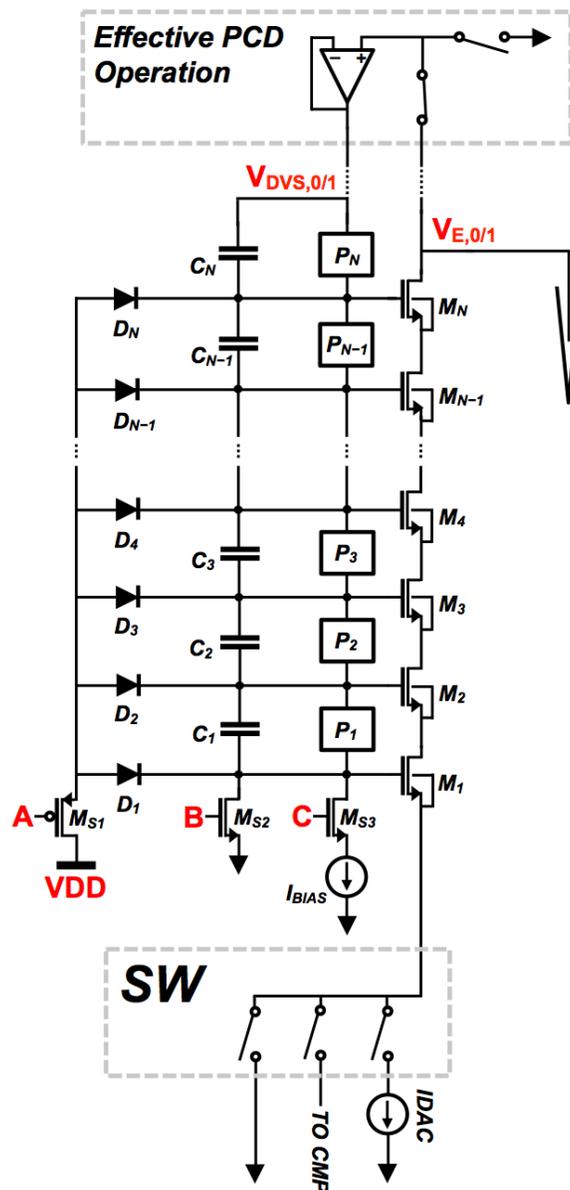
Figure 5.3. N-stage HVA circuit schematic.

5.2.1 *Circuit Overview*

Figure 5.3 also shows how an HVA circuit interfaces with other elements of the stimulus front-end; specifically its associated electrode, the positive-current driver (PCD) that controls the DVS biasing the HVA, and the set of low-side switches that is connected to the low-side HVA terminal. The effective operation of the HVA-biasing DVS, under PCD control, is modeled in Figure 5.3 using an operational amplifier (op-amp) in unity-gain feedback. Depending on the configuration of the PCD (see Chapter 3) the output of the op-amp ($V_{DVS,0/1}$) is either set to be a copy of the electrode voltage ($V_{E,0/1}$), modeling a PCD in the SUPPLY or TRACK configurations, or set to be 0V, molding a PCD in its other configurations (e.g. IDLE, DISCHARGE/RESET). With that said, it's important to note that this op-amp is only an approximative model, since due to the switched-capacitor nature of the actual DVS, the ON/OFF DVS regulation scheme used by a PCD, and the high-side switch being a diode, error between $V_{DVS,0/1}$ and $V_{E,0/1}$ will unavoidably exist during stimulus delivery. The low-side switch set can be configured to connect the low-side terminal of the HVA to ground, the current-DAC (IDAC), and/or a comparator (or to nothing at all). The circuits making up a low-side switch set are discussed in Section 5.3.

The N-stage HVA circuit itself features N capacitors, and these capacitors are sized to apply the "ideal" HVA gate-biasing function (Equation 5.1 in Section 5.1.2) to the gates of M_N through M_1. C_N, the top-most capacitor in the stack, is sized to make sure the constant-gain term, α, falls within the "safe" range of values (Equations 5.7-5.9 in Section 5.1.2) which assures V_{DS} and V_{GS} reliability throughout the HVA device stack as $V_{E,0/1}$ varies between 0V and its expected maximum value (i.e. Equation 5.6 in Section 5.1.2). Accordingly, in sizing C_N the effective capacitance in-series with it must be known, as well as the worst-case "PCD error ratio" ($V_{DVS,0/1}/V_{E,0/1}$) when the PCD controlling the HVA-biasing DVS is SUPPLY-configured (error ratio greater than 1 due to diode high-side switch) and TRACK-configured (error ratio potentially less than 1).

C_{N-1} through C_1 are sized to realize a capacitive divider with constant-increment voltage division, as to provide the "k" and "N" dependent component of the HVA gate-biasing function. Accordingly, in sizing each capacitor in this string, the lumped parasitic capacitance at the bottom plate of C_{N-1} through C_2 must be known (discussed more in Section 5.5). VDD and the turn-on voltage of diodes D_1 through D_N determine the V_{ON} of the HVA gate-biasing function, as

well as limit the minimum gate voltage of M_1 through M_N to satisfy Equation 5.29 in Section 5.1.5 (i.e. the HVA gate-biasing function for positive and negative output voltages). I_{BIAS} can be low and is used to keep the bottom of the capacitive divider network pulled down to V_{ON} as the voltage at $V_{DVS,0/1}$ increases.

In-parallel with each stacked capacitor is a sub-module that contains one of the two circuits shown in Figure 5.4 (depending on the index of the capacitor).
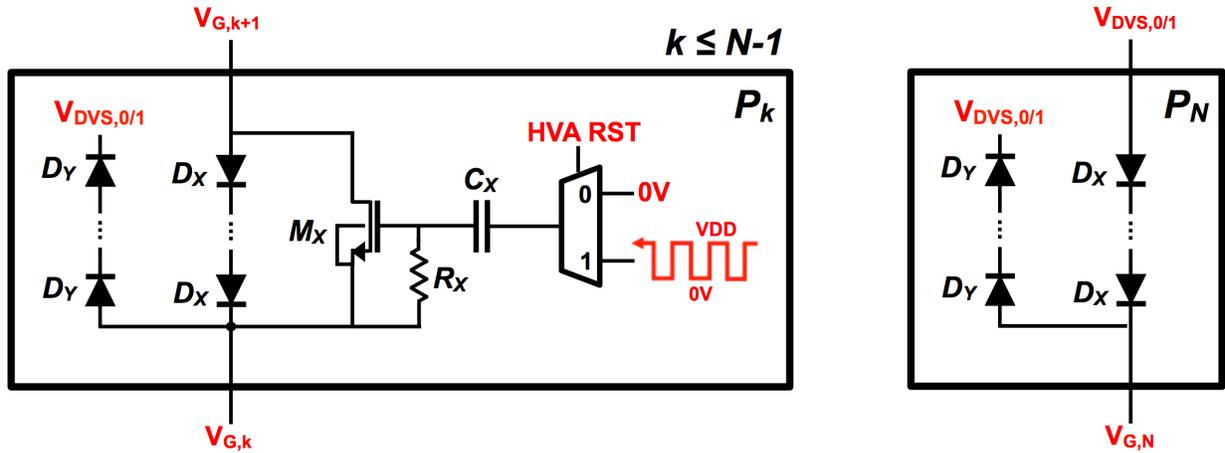
Figure 5.4. HVA sub-module schematic.

Accordingly, the M_X device in-parallel with capacitor C_1 through C_{N-1} is normally off, unless AC coupled pulses are forwarded by the multiplexer to repeatedly open and close M_X, as to discharge the in-parallel capacitor over the course a few pulse cycles. The D_X diode string and D_Y diode string (with a collective turn-on voltage around VDD) are included in each sub-module to 1) protect the HVA devices and provide crude HVA functionality if the gate-biasing function set by C_N through C_1 is significantly skewed after fabrication due to unforeseen PVT sensitivity and/or failure mechanisms (thereby allowing the rest of the stimulator, which employs two HVAs, to still be evaluated at some level); and to 2) crudely protect the HVA devices from ESD events. The functionality of these diode strings is discussed more in Section 5.5.

5.2.2 *Expected HVA Operation During Stimulus Delivery*

For an HVA to reliably apply the discussed gate-biasing function, the HVA must be placed in the right configuration, at the right point during stimulus delivery. Before the HVA is used in a high-voltage protecting capacity during the delivery of a biphasic stimulus pulse (and accordingly,

when the electrode interfacing with the HVA is known to be at low voltages), the gates of M_1 through M_N must be set to V_{ON}. Doing this requires a two-step process, beginning with the HVA being placed in the RESET configuration, in which the M_{S1} and M_{S3} switches are opened, the M_{S2} switch is closed, and C_1 through C_{N-1} are discharged via the AC-coupling of pulses to the gates of the in-parallel M_X devices (Figure 5.4). At the same time, it is assumed the DVS biasing the HVA has its output set to approximately 0V (i.e. the PCD controlling the DVS has already been cycled through its own RESET/DISCHARGE configuration).

After all of the capacitors have been discharged, the HVA can be placed in its IDLE configuration, in which I_{BIAS} (via M_{S3}) and the associated PCD are kept inactive, the M_{S2} switch is opened back up, and the M_{S1} switch is closed again, pulling the gate voltage of each HVA device up (M_1 through M_N) from 0V to V_{ON}. After the gate voltages have settled, $V_{DVS,0/1}$ should still be at approximately 0V.

Until the PCD controlling the HVA-biasing DVS is placed in the SUPPLY configuration (at which point the electrode connected to the high-side terminal of the HVA may go to voltages greater than VDD), the HVA can remain in the IDLE configuration, acting like a closed NMOS switch between the electrode (which is at a low voltage) and the low-side switch set. However, when said PCD is finally placed in the SUPPLY configuration (i.e. the PCD modeling op-amp in Figure 5.3 is configured to set $V_{DVS,0/1}$ to $V_{E,0/1}$), the HVA must be placed in its ACTIVE configuration, in which (compared to the IDLE configuration) M_{S3} is closed to have the sinking I_{BIAS} current keep the bottom plate of C_1 pulled down to V_{ON}, activating the capacitive divider network that implements the HVA gate-biasing function.

The ACTIVE HVA configuration is maintained as the PCD controlling the HVA-biasing DVS is put in the TRACK configuration (always activated subsequently to the SUPPLY configuration during biphasic stimulus pulse delivery for a given PCD), in which the electrode voltage (and the tracking DVS voltage) both fall back to low voltages. When $V_{DVS,0/1}$ and $V_{E,0/1}$ in Figure 5.3 finally return to low voltages (i.e. when the associated PCD is once again placed in a configuration other than SUPPLY or TRACK), then the HVA can be placed in the IDLE configuration for the remaining duration of the delivery of a single biphasic stimulus pulse. Then the cycle can repeat, with the HVA placed in the RESET configuration at sometime between the delivery of consecutive biphasic stimulus pulses. More details pertaining to the bulk-CMOS

implementation of the HVA circuit (e.g. voltage limitations, device sizing, ESD protection) are provided in Section 5.5.

5.3   LOW-SIDE SWITCH SET DESCRIPTION

A low-side switch set is used to connect the voltage-protected low-side terminal of an HVA to the current-DAC (IDAC), a comparator (dropout detecting and/or ε_{SUPPLY} generating), and ground, enabling the stimulus driving functionality of the proposed stimulator front-end (see Chapter 3). Figure 5.5 shows the schematic of a low-side switch set, which interfaces with a single HVA; this implementation assumes dropout detection and ε_{SUPPLY} generation is performed by the same comparator (for both PCDs).
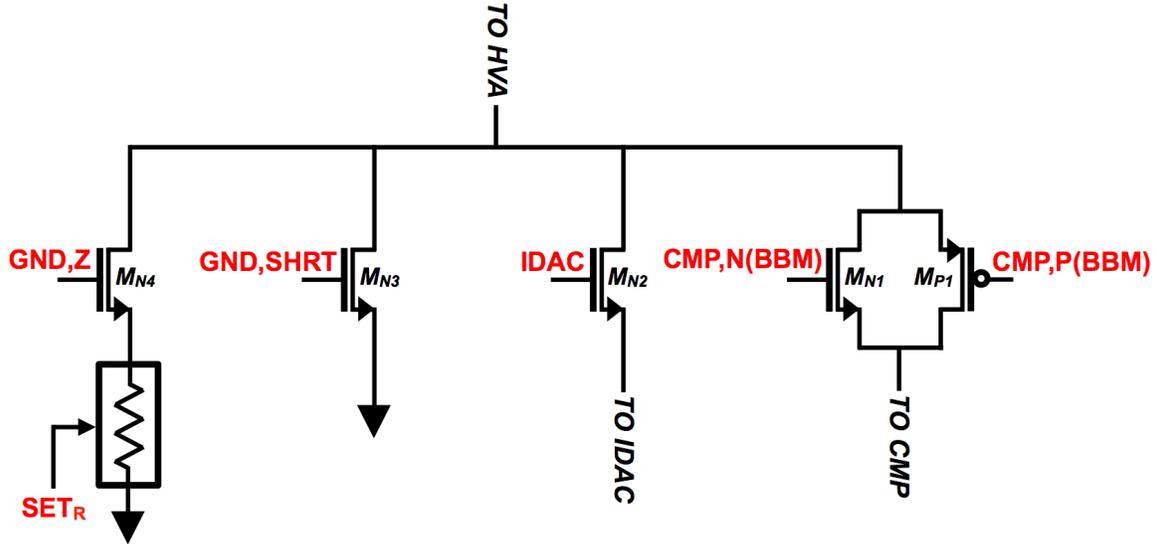
Figure 5.5. Low-side switch set schematic.

As shown in Figure 5.5, two different switches are available to connect the low-side of an HVA to ground. M_{N3} (a large device), controlled by the GND,SHRT digital control signal, can be activated to provide a low-impedance pathway; alternatively M_{N4}, which is in-series with a digitally controlled variable resistor (i.e. an RDAC), can also be employed (e.g. to limit the discharge rate of the electrode-tissue-interface during electrode shorting). Since the value of the variable resistor shouldn't need to be dynamically adjusted during stimulus delivery, the requisite RDAC performance is low (aside from the number of bits and resistance values the designer desires), and accordingly a wide variety of implementations can be used to realize it.

M_{N2} should have the same sizing as M_{N3}, as to (when activated) provide a low-impedance path to the sinking IDAC.

The comparator switch is implemented with complementary NMOS (M_{N1}) and PMOS (M_{P1}) devices. A CMOS switch is used because of the large voltage ripple that may appear at the low-side terminal of the HVA during stimulus delivery (due to the operation of a SUPPLY-configured PCD). Considering this voltage ripple and the high-impedance input of the comparator, the CMOS switch provides more uniform conduction between the HVA low-side terminal and the comparator input across the worst-case range of low-side terminal voltages.

Because the same comparator is used for both dropout detection and ε_{SUPPLY} generation (by both PCDs), break-before-make (BBM) switching is required between the CMOS comparator switches of the two low-side switch sets (0 and 1) employed by the proposed stimulator front-end (see Chapter 3); else, there is chance during stimulus delivery the two CMOS comparator switches could inadvertently be closed at the same time (albeit briefly) and short the two electrodes together. Figure 5.6 shows the digital circuitry required to realize said BBM control, where CMP_0 and CMP_1 are the active-high control signals of the comparator switch in the 0 and 1 low-side switch sets, respectively.
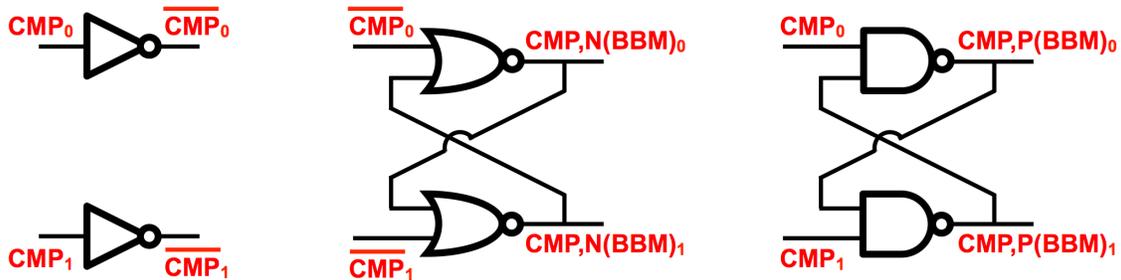
Figure 5.6. Break-before-make (BBM) control circuitry for comparator switches of low-side switch sets 0 and 1.

5.4 SUMMARY OF DIGITALLY SET CONFIGURATIONS

5.4.1 *High-Voltage Adapter (HVA)*

The HVA has four different configurations, which can be digitally set using the control signals A, B, C, and HVA RESET (see Figure 5.3 and Figure 5.4 in Section 5.2); a summary of said configurations is provided in Table 5.1. The 0/1 binary value of each control signal listed in Table 5.1 corresponds to 0V/VDD, where VDD is less than or equal to the voltage rating of the devices used to implement the HVA circuit.

Table 5.1. High-Voltage Adapter (HVA) Configuration Summary

Configuration #	Description	HVA Control Signals			
		A	B	C	HVA RESET
0	OFF	1	1	0	0
1	IDLE	0	0	0	0
2	ACTIVE	1	0	1	0
3	RESET	1	1	0	1

The IDLE, ACTIVE, and RESET configurations are described in detail in Section 5.2.2. In the OFF configuration the gate of the bottom HVA device is set to ground and power is shut off from the circuit (both VDD and I_{BIAS}). However, while the HVA can be placed in the OFF configuration, it is not a necessary HVA configuration for biphasic stimulus delivery.

5.4.2 *Low-Side Switch Set (SW)*

The different configurations of a low-side switch set are characterized as certain switches being on and conducting and others being off and non-conducting. Collectively, the 7 different configurations listed in Table 5.2 provide the functionality required by the stimulator front-end proposed in Chapter 3, as well as enable additional functionality, like being able to use the dropout detecting comparator during discharging events to detect when an electrode voltage has fallen to low levels (i.e. Configuration 5 and Configuration 6 in Table 5.2). Table 5.2 assumes break-before-make (BBM) switching is used to control the comparator switch, and therefore the control signals listed in the table correspond to those shown in Figure 5.5 and Figure 5.6 (Section 5.3). The 0/1 binary value of each control signal listed in Table 5.2 corresponds to 0V/VDD,

where VDD is less than or equal to the voltage rating of the devices used to implement the low-side switch set and BBM circuits.

Table 5.2. Low-Side Switch Set (SW) Configuration Summary

Configuration #	Description	SW Control Signals			
		GND,Z	GND,SHRT	IDAC	CMP
0	HIGH Z	0	0	0	0
1	GND VIA SHRT	0	1	0	0
2	GND VIA Z	1	0	0	0
3	CMP ONLY	0	0	0	1
4	CMP, IDAC	0	0	1	1
5	CMP, GND VIA SHRT	0	1	0	1
6	CMP, GND VIA Z	1	0	0	1

5.5 ADDITIONAL IMPLEMENTATION NOTES AND CONSIDERATIONS

5.5.1 *HVA Capacitor Sizing Methodology*

At the bottom-plate of capacitors C_{N-1} through C_2 in the N-stage HVA circuit (Figure 5.3 in Section 5.2), parasitic capacitance will unavoidably exist due to the presence of potentially large HVA devices, as well as C_X, M_X, and the diode strings in the HVA sub-modules (Figure 5.4 in Section 5.2). However, for a given α, the lumped parasitic at each bottom-plate node should be approximately the same (defined as C_{PAR}). Accordingly, after estimating C_{PAR} and choosing the value of C_1, the recursive technique shown in Equation 5.30 can be used to find the required values of C_2 through C_{N-1} to make the resulting capacitive divider have constant-increment division (as required by the HVA gate-biasing function). C_1 should be chosen to be sufficiently large so that if C_{PAR} is varies slightly from the estimated value (due to non-linear contributions and/or PVT variation), the resulting division ratio at each bottom-plate node won't significantly deviate from constant-increment division. However, form-factor must also be considered in sizing C_1, since as k increases, the capacitance C_k required by Equation 5.30 also increases.

$$C_k = (k-1)C_{EQ(k-1)} \quad \text{where} \quad C_{EQ(k-1)} = \begin{cases} C_{PAR} + C_1 & \text{for } k = 2 \\ C_{PAR} + \frac{C_{k-1}C_{EQ(k-2)}}{C_{k-1}+C_{EQ(k-2)}} & \text{for } k > 2 \end{cases} \quad (5.30)$$

With values for C_1 through C_{N-1} determined, C_N can then be sized to set/adjust α of the HVA gate-biasing function (as to account for the worst-case PCD error between DVS and electrode voltages during stimulus delivery).

5.5.2 *PCD Error*

In recognizing C_N can only be used to reduce the constant-gain term (α) of the HVA gate-biasing function, a PCD error ratio (i.e. $V_{DVS,0/1}/V_{E,0/1}$) that is significantly less than one is problematic, since such could not be offset by C_N sizing while potentially pushing α outside the "safe" region of values (Equations 5.7-5.9 in Section 5.1.2). Accordingly, precautions must be made in designing the various blocks of a PCD (e.g. PCD loop delay, comparator offset, etc.) to make sure that PCD error can be corrected through C_N sizing, as to produce a value of α that assures device reliability, during both SUPPLY-configured and TRACK-configured operation.

However, if the observed PCD error ratio does push α below α_{min} (Equation 5.8 in Section 5.1.2), HVA reliability can still be assured through increasing N. Although increasing N will increase α_{min}, $V_{OUT(max)}$ (Equation 5.6 in Section 5.1.2) will also be increased. Accordingly, by pushing $V_{OUT(max)}$ well past the maximum voltage the HVA is actually expected to interface with at the electrode, then even if α is less than α_{min} (i.e. devices operate more in the saturation region in moving up the HVA stack), the V_{DS} of M_N (and all lower devices) can still be made to stay within the device ratings across the expected electrode voltage range (but such must be verified with simulations).

5.5.3 *HVA Voltage Limitations*

With M_N of the HVA being a DNW NMOS device (with the DNW tied to the drain) the maximum voltage an HVA can interface with at the electrode is limited by the reverse breakdown voltage of the p-substrate-to-deep-n-well (PSUB/DNW) junction (this breakdown voltage limits the DVS output voltage as well).

Large voltages (i.e. greater than VDD) can also be observed across the D_1 through D_N diodes (when reverse-biased) and the C_X capacitors (in HVA sub-modules up to $k = N - 1$) during stimulus delivery. Accordingly, D_1 through D_N must be implemented with a diode structure that exhibits an adequately high reverse breakdown voltage, such as the lowly doped p-

well-to-deep-n-well (PWELL/DNW) junction; likewise, C_X should be implemented with a capacitor structure featuring sufficient voltage tolerance (i.e. not a MOS-capacitor).

5.5.4 D_X and D_Y Diode Strings and ESD Protection

Although C_N through C_1 should properly implement a "safe" HVA gate-biasing function if the sizing methodology described in Section 5.5.1 is utilized, the HVA circuit has thus far not been verified with measurements, and accordingly unforeseen PVT sensitivity and/or failure mechanisms could feasibly be observed in a fabricated HVA circuit, resulting in an undesired gate-biasing function being applied to the gates of M_N through M_1. However, if such were to occur, causing the divide function implemented by C_N through C_1 to be significantly skewed, the D_X diode string (Figure 5.4 in Section 5.2) in-parallel with each capacitor would ultimately limit the maximum voltage that can be built across it to its collective turn-on voltage (which should be set to be less than or equal to the VDD-rating of the HVA devices). Accordingly, when the HVA-biasing DVS is being controlled by a PCD in the SUPPLY configuration (i.e. the electrode voltage is expected to rise) the D_X strings at least are able to crudely protect M_1 through M_N of an N-stage HVA from V_{DS} overstress.

However, after the PCD controlling the HVA-biasing DVS is placed in the SUPPLY configuration, it is then always placed in the TRACK configuration (during stimulus delivery), as to force its DVS to track the voltage of the electrode on the same side of the H-bridge back down to sub-VDD levels. Accordingly, each capacitor, C_N through C_1, has a D_Y diode string (with a collective turn-on voltage approximately equal to the VDD-rating of the HVA devices) between its bottom plate and the DVS bias voltage (Figure 5.4). This auxiliary circuit therefore allows the gate voltage of M_1 through M_N to be pulled down by the DVS if the difference between a gate voltage and the DVS voltage gets exceedingly large, crudely protecting the HVA devices from V_{GS} overstress as the DVS and electrode voltages return to low levels.

The D_Y and D_X diode strings also help in protecting the HVA from ESD events (both positive and negative). Although not shown in Figure 5.3 (Section 5.2), other ESD protecting diode strings with turn-on voltages of approximately the VDD-rating of the HVA devices exist in the N-stage HVA circuit in the following locations: 1) in-parallel with devices M_1 through M_N (with effective n-terminal connected to the source); 2) between $V_{E,0/1}$ and $V_{DVS,0/1}$ (with effective n-terminal connected to the DVS); 3) between the bottom-plate of C_1 and ground (with effective

n-terminal connected to ground); and 4) in-parallel with the low-side switch set (with effective n-terminal connected to ground). Accordingly, even if chip power and/or I_{BIAS} are not active, if a large positive change in voltage were to applied to the electrode (previously at low voltages), the gate voltages of M_1 through M_N would quickly rise with the drain and source voltages, as to prevent large V_{GS} and V_{DS} voltages from being developed across any one device. Likewise, if a large negative change in voltage were to be applied to the electrode (previously at a high voltage), each gate voltage would be quickly pulled down, no matter the state of I_{BIAS} and/or chip power.

Absolute positive and negative electrode voltages, during an ESD event, are crudely limited by the reverse breakdown voltage and forward turn-on voltage of the PSUB/DNW junction, respectively.

5.5.5 *VDD, V_{ON}, and Circuit Device Ratings*

V_{ON} of the HVA gate-biasing function is set to VDD minus a diode drop. Accordingly, VDD and V_{ON} establish the voltage ratings required of the transistors used to implement both the HVA and low-side switch set. For the HVA devices, this device rating is the maximum "VDD" that can be used in assessing the maximum electrode voltage the HVA can interface with (i.e. $V_{OUT(max)}$ from Equation 5.6 in Section 5.1.2).

5.5.6 *Glitch-Free and Synchronized Digital Control Signals*

The digital control signals used to configure an HVA and a low-side switch set should be the direct or buffered output of dynamic logic blocks (e.g. D-flip-flops) that are synchronized to a system clock, as to prevent transient glitches due to static logic from being expressed in the control signals during configuration transitions.

5.6   POST-LAYOUT SIMULATIONS

A 7-stage HVA has been designed in the TSMC 65nm GP CMOS process. The 2.5V devices of the process are used to implement all HVA devices (Figure 5.3 and Figure 5.4 in Section 5.2) as well as the low-side switch set and break-before-make (BBM) control circuits interfacing with the low-side terminal of the HVA (Figure 5.5 and Figure 5.6 in Section 5.3); accordingly, level shifters [25] are used to interface these two circuit blocks with low-voltage, LVDD-powered (1V nominal) digital control circuitry.

V_{ON} of the HVA gate-biasing function is set to 2.5V minus a diode drop, and M_1 through M_7 are of equal W and L and sized to provide a collective minimum drain-to-source voltage of approximately 200mV at 2mA drain current. The gate-biasing function applying capacitors $\{C_1, C_2, C_3, C_4, C_5, C_6, C_7\}$ are set to approximately $\{$1pF, 1.28pF, 1.84pF, 2.68pF, 3.8pF, 5.2pF, 10pF$\}$; these values are set in accordance to an observed parasitic capacitance of approximately 280fF at the gates of M_1 through M_7. The HVA reset pulse signal is a 13.56MHz clock signal, and C_X and R_X of the P_1 through P_6 HVA sub-modules are set to approximately 110fF and 120kΩ, respectively. Each D_X diode is implemented using a p-well-to-deep-n-well (PWELL/DNW) junction, which is simulated to have a sufficiently high reverse breakdown voltage for 0V to 12V HVA operation. I_{BIAS} is set to 2μA, nominally.

Figure 5.7 demonstrates the post-layout performance of the described HVA (and low-side switch set) in terms of applying the gate-biasing function to M_1 through M_7 when the electrode and DVS voltages are equal and varied between 0V and 12V (with 5μs rise/fall-time). Figure 5.7 also shows how the HVA is digitally configured versus time to provide the illustrated functionality (where the provided configuration numbers correspond to Table 5.1 in Section 5.4.1); accordingly, if the RESET configuration is activated (for only a short time interval) between consecutive large voltage variations at the electrode (and DVS), consistent and reliable HVA performance can be assured over the course of long-term operation. The configuration of the low-side switch set is also varied versus time in the Figure 5.7 simulation from being high-Z to being a short to ground, as to demonstrate the HVA operating at zero drain current and maximum drain current. The low-side switch set configuration numbers shown in Figure 5.7 correspond to Table 5.2 in Section 5.4.2.
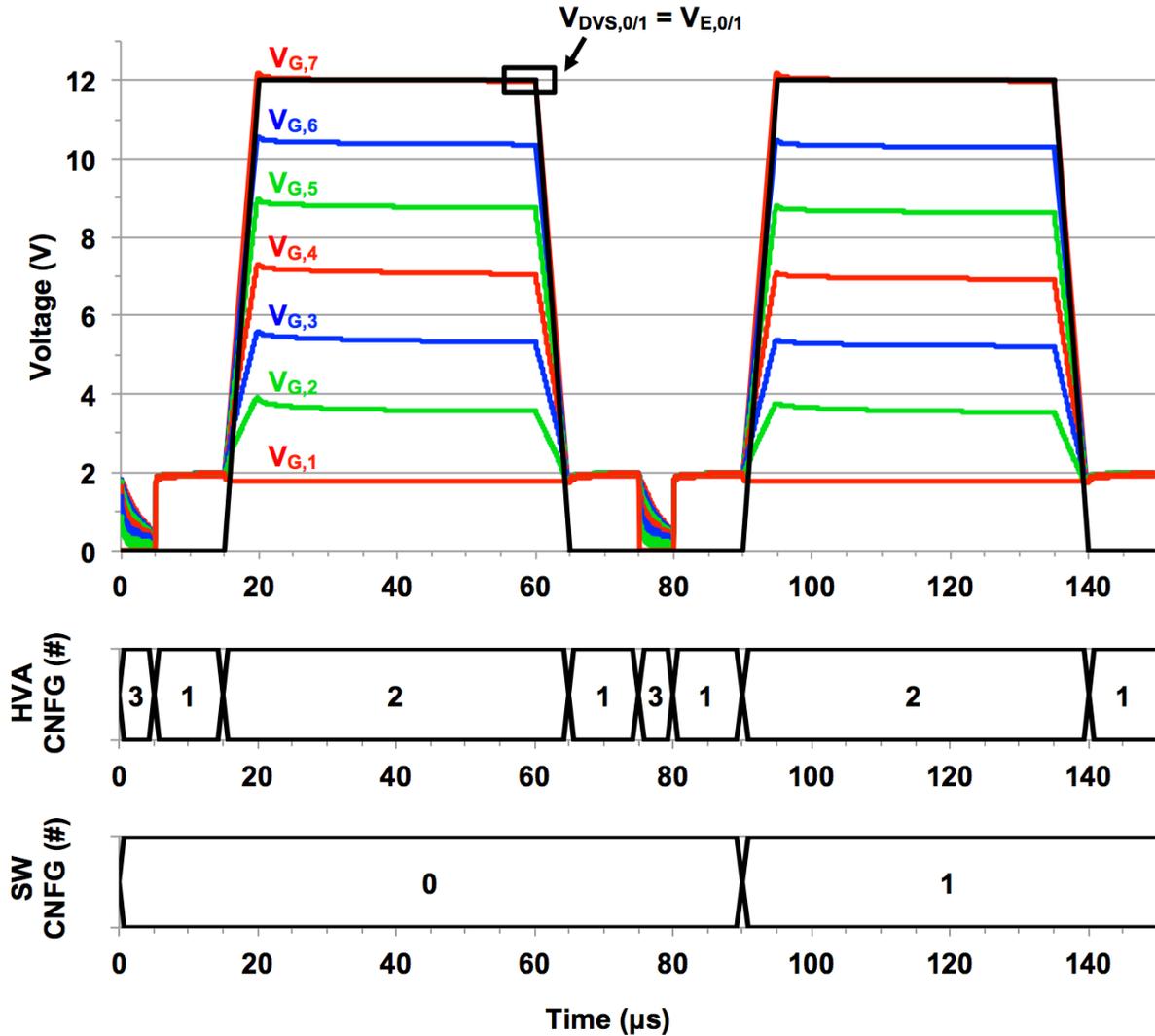
Figure 5.7. Transient post-layout simulation of 7-stage HVA showing gate voltages of devices M_1 through M_7; $V_{DVS,0/1} = V_{E,0/1}$.

The observed ranges of V_{GS}, V_{DS}, and V_{DG} for M_1 through M_7 during the Figure 5.7 simulation (when the HVA is in the ACTIVE configuration) are provided in Figure 5.8, which shows that all terminal-to-terminal voltages across the HVA device stack stay within the "safe" $-2.5V$ to $+2.5V$ range. Furthermore, Figure 5.9 provides the V_{GS}, V_{DS}, and V_{DG} ranges observed during a similar HVA simulation in which the DVS voltage is 0.7V greater than the electrode voltage, as to better demonstrate the voltage-protection functionality of an HVA when the PCD setting the HVA-biasing DVS voltage is in the SUPPLY configuration. Likewise, Figure 5.10 provides the V_{GS}, V_{DS}, and V_{DG} ranges observed during an HVA simulation in which the DVS voltage is 1.8V less than the electrode voltage, as to demonstrate the voltage-protection

functionality of the HVA if there is significant negative overshoot when the PCD setting the HVA-biasing DVS voltage is in the TRACK configuration.
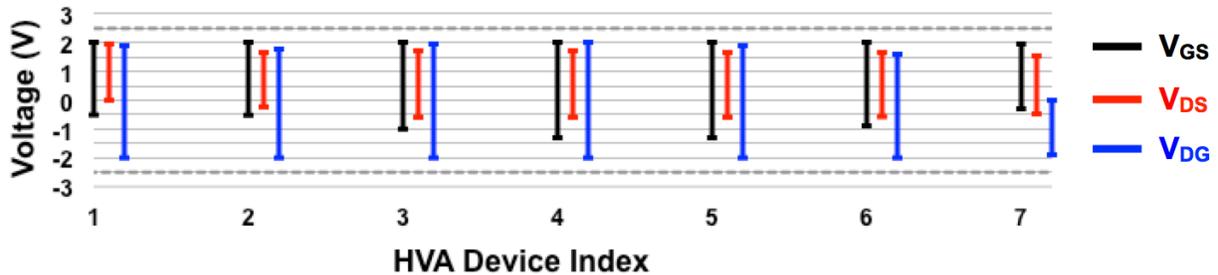
Figure 5.8. Observed terminal-to-terminal voltages of HVA devices (M_1 through M_7) during transient simulation (I_D set to both zero and maximum); $V_{DVS,0/1} = V_{E,0/1}$ with $V_{E,0/1}$ varied between 0V and 12V.
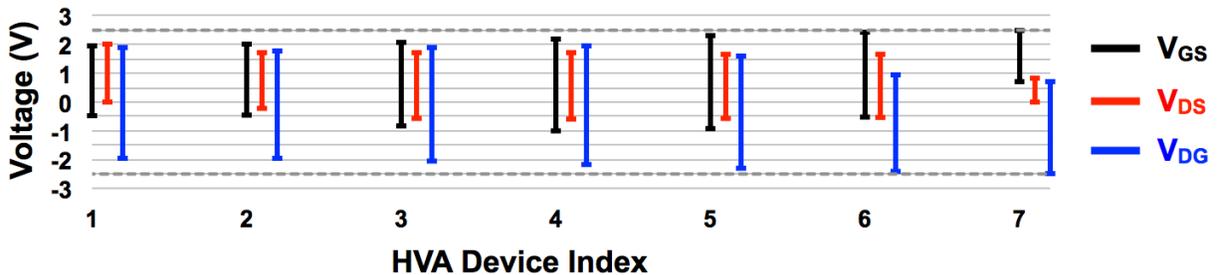
Figure 5.9. Observed terminal-to-terminal voltages of HVA devices (M_1 through M_7) during transient simulation (I_D set to both zero and maximum); $V_{DVS,0/1} = V_{E,0/1} + 0.7V$ with $V_{E,0/1}$ varied between 0V and 11.3V.
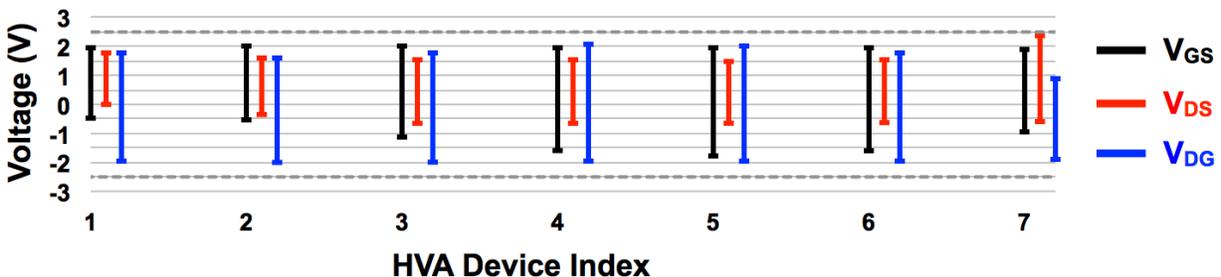
Figure 5.10. Observed terminal-to-terminal voltages of HVA devices (M_1 through M_7) during transient simulation (I_D set to both zero and maximum); $V_{DVS,0/1} = V_{E,0/1} - 1.8V$ with $V_{E,0/1}$ varied between 0V and 12V.

Chapter 6. IN-VIVO EXPERIMENTS USING PROTOTYPE STIMULATION SYSTEM

The integrated stimulator topology presented in Chapter 3 employs an H-bridge-style front-end. In general, very few H-bridge-based stimulators, of any topology and implementation, have been demonstrated *in-vivo*. Furthermore, groups that have demonstrated such [13] have only disclosed measurements associated with a limited number of electrode configurations (i.e. electrode type and placement). Accordingly, with a lack of data in the literature, the *in-vivo* current-regulating ability of an H-bridge-based stimulator could be more thoroughly validated through further demonstrations and measurements, since active and return electrode placement (and impedance) can widely vary across neural stimulation applications.

Additionally, as discussed in Chapter 4, the p-substrate-to-deep-n-well (PSUB/DNW) junction of a bulk-CMOS process restricts the maximum output voltage (V_{MAX}) a dynamic voltage supply (DVS) circuit can generate; therefore, if the stimulator topology proposed in Chapter 3 were to be integrated in a bulk-CMOS process, the DVS V_{MAX} would limit the voltage compliance of the stimulator front-end, and whether or not the resulting compliance would be high enough for "real-world" neural stimulation applications is a valid concern.

Accordingly, a board-level prototype stimulator, which employs a simple sink-regulated H-bridge front-end, has been realized to 1) investigate potential uses for the proposed integrated stimulator (considering the compliance limits associated with an integrated implementation), and 2) to verify the current-regulating ability of an H-bridge stimulator *in-vivo* across a variety of electrode configurations. The high-level design of the prototype stimulation system, and the subsequent *in-vivo* (rat) experimental trials the prototype was used in are the focus of this chapter.

6.1   PROTOTYPE DESCRIPTION

The prototype stimulation system is designed for biphasic, constant-current stimulation, and employs a standard sink-regulated H-bridge front-end with a single, static HVDD. The H-bridge front-end portion of the system is implemented on a custom printed circuit board (PCB). The switches of the H-bridge front-end are implemented using discrete, high-voltage-tolerant components (Maxim MAX6413EPE Quad, SPST Analog Switch), which can be set ON/OFF using low-voltage digital signals; for a worst-case, completely capacitive electrode-tissue-interface impedance (Z_E), these discrete switches allow HVDD to be set as high as 20V, providing approximately ±20V stimulator compliance. Bench power supplies are used to provide HVDD and other necessary voltage rails; additionally, with the present version of the prototype system, an external bench current source (Keithley 236 Source Measure Unit) is used to regulate the stimulus current at adjustable, and widely ranging levels. A separate microcontroller unit (Texas Instruments MSP430 LaunchPad) is used to control the H-bridge front-end, turning its switches ON and OFF with precise timing, as to deliver biphasic, charge-balanced stimulus with programmable pulse-width, interphase delay, and pulse frequency.

The front-end interfaces with two electrodes (active and return). To assure charge balance and to protect the tissue in the case of an electronic fault, large blocking capacitors are included in-series with the electrodes, providing capacitive isolation between the electrode-tissue-interface and the stimulation electronics. Test-points exist on the front-end-circuitry-side of the blocking capacitors for oscilloscope voltage measurements. Additionally, in-series with each blocking capacitor (and on the front-end-circuitry-side of said capacitors) is a current-sense resistor, which can be used to gauge electrode current during stimulus delivery. The fabricated stand-alone DVS chip (introduced in Chapter 4) is not used, in any way, within this prototype system.

A simplified block diagram of the entire prototype system is given in Figure 6.1, and a photo of the present version of the H-bridge front-end PCB, with its accompanying microcontroller unit, is shown in Figure 6.2.
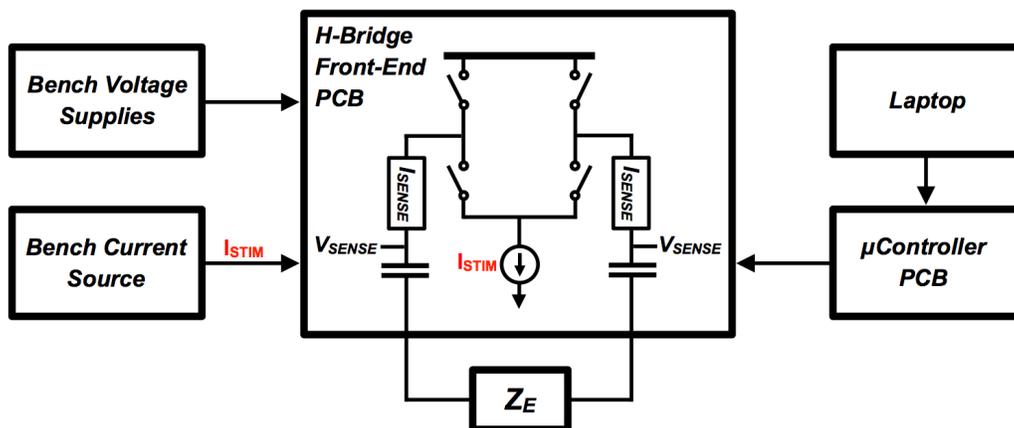
Figure 6.1. Simplified block diagram of prototype stimulation system.
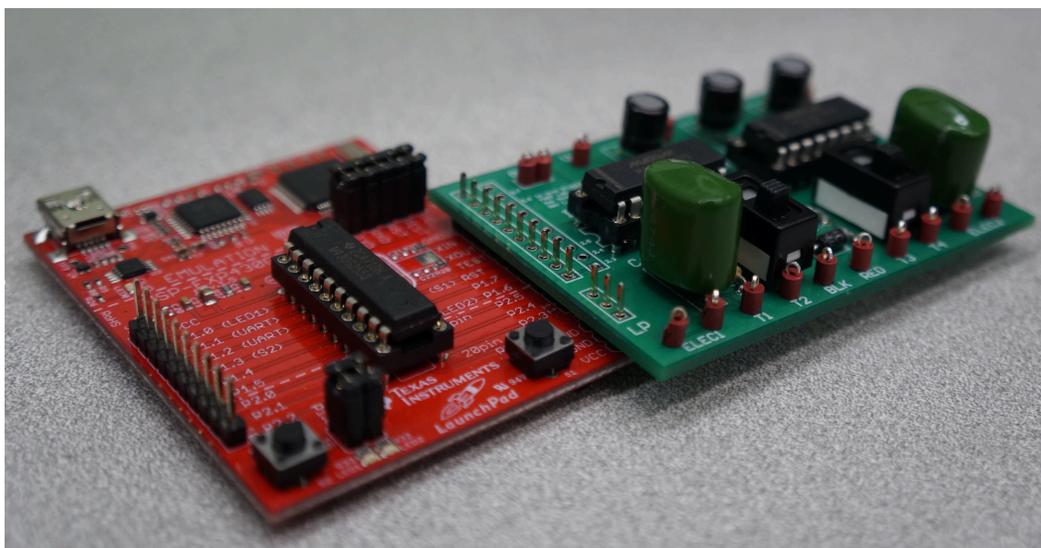
Figure 6.2. PCB components of prototype stimulation system; (LEFT) Texas Instruments MSP430 LaunchPad microcontroller unit; (RIGHT) H-bridge front-end featuring high-voltage switches, electrode voltage/current probe points, and series blocking capacitors.

6.2   EXPERIMENTAL SETUP

A diagram illustrating the experimental setup is shown in Figure 6.3. Two rats, previously surgically implanted with several electrode configurations (subdural cortical, intracortical, intraspinal, and intramuscular) were stimulated while moving freely about an observation area, with each electrode configuration arranged to evoke wrist-extensor movement. The prototype stimulator was connected to implanted electrodes using a tethered cable. A 300µm multi-stranded, stainless steel (SS) wire was used for the return electrode, in all of the configurations, and the active electrode was either a 300µm multi-stranded SS wire (intramuscular, subdural-cortical) or a 30µm platinum/iridium (Pt/Ir) wire (intraspinal, intracortical).
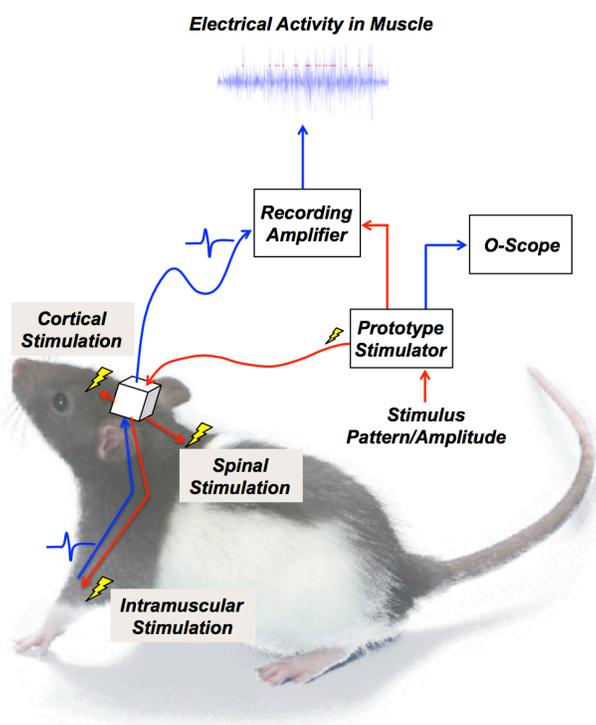
Figure 6.3. Diagram of *in-vivo* experimental setup.

For the intracortical and intraspinal configurations, the active electrode and the return electrode were distantly placed from one another, with only the active electrode close to the targeted neural tissue. For the intramuscular configuration, the active electrode and the return electrode were placed near the location of the targeted neural tissue. Two subdural cortical configurations were available, one with a distant return, and the other using active and return electrodes both interfacing with subdural cortical tissue.

Electro-myographic (EMG) responses in the targeted muscle and near the spinal cord (latter for subdural cortical and intracortical stimulation) were recorded during stimulus delivery (using a "capture trigger" generated by the stimulator prototype). A digital oscilloscope was used to probe electrode voltages and currents during stimulus delivery (via probe points and current sensing units within the stimulator prototype) to observe and assess the current-regulation performance of the H-bridge, the impedance profile of Z_E, and the requisite compliance levels of the different investigated stimulation applications.

The HVDD of the stimulator prototype was set sufficiently high, as to have approximately the same compliance as the integrated stimulation front-end proposed in Chapter 3, if such were to be implemented in a modern bulk-CMOS technology (i.e. 65nm TSMC GP CMOS). Accordingly, the base-level HVDD was set to 11V, giving the prototype stimulation system approximately ±11V compliance; if needed/desired, the HVDD of the prototype could be increased during the course of an experiential trial.

The patterns of the delivered stimulus varied from trial-to-trial, but stimulus pulse-width (i.e. the duration of each phase of a biphasic pulse) was kept constant at 200μs. At the beginning of each stimulus trial, the stimulus amplitude was set low (e.g. 10μA) and was steadily increased in small, fixed increments until the wrist-extensor of the rat was observed to respond, either visually or via EMG recordings. Stimulus trials for a given rat, electrode-configuration combination were terminated when the rat did not respond by a pre-determined maximum stimulus level, or when the voltage required for stimulation exceeded the capabilities of the prototype system. All phases of the described experiments were overseen by individuals certified by the University of Washington for such procedures.

6.3   RESULTS AND OBSERVATIONS

Sufficient stimulus current was delivered to the subdural cortical, intraspinal, and intramuscular electrode configurations to evoke forelimb or neck contractions (with electrode voltages less than ±11V). Figure 6.4a shows the measured electrode voltage during response-evoking stimulation for the subdural cortical electrode configuration (with distant return) and the intramuscular electrode configuration; Figure 6.4b shows the recorded EMG response during the delivery of the intramuscular stimulus. The measured electrode voltages during intraspinal stimulation were low (approximately ±1V or so), while the requisite compliance for the investigated intracortical electrode configuration was observed to exceed ±11V by a considerable margin.
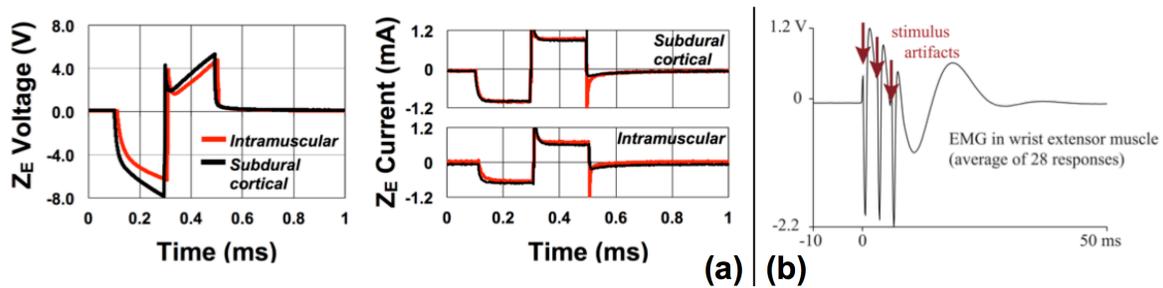
Figure 6.4. *In-vivo* results for 200µs pulse-width, biphasic, constant-current stimulation using prototype stimulation system: (a) Z_E voltage and active/return current (switching transients result of on-board parasitics) for 710µA intramuscular stimulation (3@300Hz repeated at 1Hz), and for 1000µA cortical stimulation (5@300Hz repeated at 1Hz); (b) wrist-extensor EMG recordings during 710µA intramuscular stimulation.

In Figure 6.4a, the return and active electrode current, corresponding to the Figure 6.4a voltage measurements, are also provided. Accordingly, an H-bridge-based front-end appears to be able to regulate the stimulus through both electrodes, *in-vivo*, regardless of the "distance" between active and return electrodes. Figure 6.4a also shows that the response-eliciting current amplitudes associated with these particular neural stimulation applications are quite high (i.e. around 1mA). Lastly, the frequency-dependent nature of the Figure 6.4a voltage waveforms supports the need for the "electrode-invariant" stimulator topology proposed in Chapter 3. However, a portion of the Z_E capacitance suggested by the observed voltage waveforms can be attributed to the blocking capacitors used by the prototype stimulator (i.e. the electrode voltage measurements were taken on the front-end-circuitry-side of the blocking capacitors).

Chapter 7. HIGH-VOLTAGE COMPLIANT, ELECTRODE-INVARIANT, BULK-CMOS STIMULATOR CHIP

A complete neural stimulator front-end, employing the electrode-invariant H-bridge topology discussed in Chapter 3, has been designed in the TSMC 65nm GP CMOS process. To be potentially useful in a wide array of neural stimulation applications (e.g. intraspinal, subdural cortical, intramuscular, etc.) this stimulator integrated circuit (IC) is designed to deliver 50μA to 2mA biphasic, constant-current stimulus; across this stimulus current range, post-layout simulations show the front-end achieves approximately ±11V compliance.

In Section 7.1, an overview of the chip is given, and in Section 7.2 the control schema employed by the integrated system is discussed in detail. Then, in Section 7.3, post-layout simulations are provided which demonstrate the current range and voltage compliance of the integrated stimulator, as well as the ability of the chip to drive biphasic, constant-current stimulus through a wide range of electrode-tissue-interface impedances (from purely resistive to purely capacitive). Based on these simulation results, a projected comparison to the state-of-the-art is provided in Section 7.4, followed by a brief discussion on the observed positives and negatives of this work, and how some of these negative can be potentially mitigated with future research.

7.1   CHIP OVERVIEW

A block diagram of the stimulator chip is given in Figure 7.1. The electrode-interfacing part of the chip is divided up into two symmetric modules (denoted "0" and "1"), with each module corresponding to one side of the H-bridge front-end topology discussed in Chapter 3. Each H-bridge module has a connection to an electrode, and electrode orientation during stimulation (i.e. the active/return designation) is set by a bit read from the shift register (i.e. A/R in Figure 7.1).
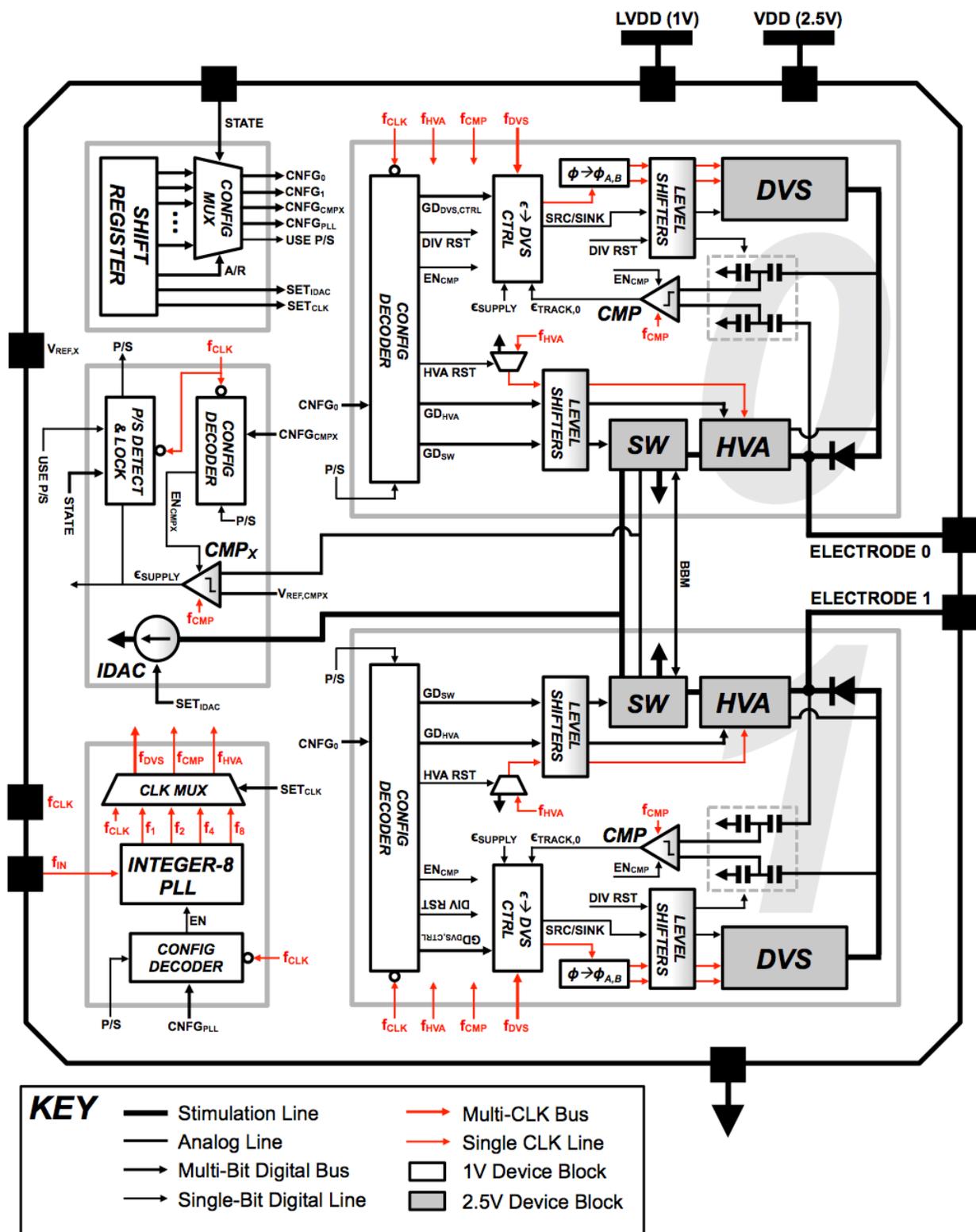
Figure 7.1. Block diagram of chip; a high-voltage compliant, bulk-CMOS stimulator front-end.

Figure 7.1 shows the duel supply input required by the chip (LVDD and VDD), and how the chip is partitioned in terms of 1V and 2.5V devices (both available without any extra processing steps in the 65nm CMOS process the chip is designed in). The DVS and HVA of each identical H-bridge module are implemented with 2.5V devices to minimize the number of stages in each block; because the HVAs are implemented using 2.5V devices, each low-side switch set (SW) is as well. To allow low-voltage devices to be used to implement the rest of the chip (e.g. digital control, frequency synthesis, etc.), some blocks within the H-bridge modules operate at the LVDD/VDD interface and incorporate both 1V and 2.5V devices (i.e. the level shifters [25], current-DAC, and comparators). VDD is nominally 2.5V, but can be reduced, especially if the chip is not being used to deliver full-scale 2mA stimulus. LVDD is nominally 1V.

The DVS implementation used by the chip has 8 stages, and can deliver 2mA stimulus at an output voltage of 12V when VDD = 2.5V (with 5% worst-case variation) and the frequency of the input pulse signal (Φ) is less than the maximum operating frequency of 108.48MHz. The specifics of this DVS implementation are summarized in Chapter 4, with post-layout simulation results provided. Likewise, the HVA and low-side switch set implementations used by the chip are summarized in Chapter 5, with post-layout simulation results also provided. The low-side switch of a given H-bridge module provides the set of the other module with the OFF/ON state of its comparator switch (via pair of 0V to VDD digital signals), to enable break-before-make (BBM) switching.

The chip utilizes a total of 3 clocked comparators, each having the same design, which demonstrates a common-mode input range down to 0V, a 2.5V tolerant (and low leakage) front-end, and a 0V to LVDD output; the maximum clocking rate applied to any of the comparators is 108.48MHz. Each front-end module features a dedicated comparator, which is used for feedback error detection by the associated positive-current driver (PCD) when in the TRACK configuration; the third comparator, denoted CMP_X, is shared by both PCDs for feedback error detection when in the SUPPLY configuration, and is also used for current-DAC dropout detection; the low-voltage reference connected to the positive terminal of CMP_X ($V_{REF,CMPX}$) is generated off-chip. When the clocked comparators are not in use, each can be readily disabled to lower power consumption.

A binary weighted current-DAC (IDAC), which employs an active-cascode topology, is used to regulate the stimulus current delivered by the chip. The minimum and maximum allowed

IDAC output levels are 50μA and 2mA, respectively, and an 8-bit design allows stimulus current to be adjusted in 10μA increments (unused/invalid IDAC codes are due to DVS and PCD performance limitations). The IDAC can be controlled using low-voltage digital signals (0V to LVDD), and the IDAC output can safely handle 2.5V.

An on-chip, analog, interger-8 phase-locked loop (PLL) generates the "high-frequency" clocks used by the comparators, DVSs, and HVAs. The PLL is designed to take a 13.56MHz (ISM-band center frequency) input (f_{IN}), and provide an output frequency of $8f_{IN}$ (f_8); frequency taps for $4f_{IN}$ (f_4), $2f_{IN}$ (f_2), and $1f_{IN}$ (f_1) are also provided by buffering-out the intermediate signals of the PLL frequency divider. Based on the clock setting bits (SET_{CLK}) loaded to the shift register, these four clocks, as well as the system clock (f_{CLK}), are digitally multiplexed to assume block-specific clock roles: f_{CMP} is the sampling clock used by all three comparators when enabled; f_{DVS} is a multi-clock bus, with a dedicated clock for each PCD configuration, i.e. f_{DVS} = $\{f_{DVS(I)}, f_{DVS(2)}, f_{DVS(3)}, f_{DVS(4)}\}$ (see Table 3.1 in Chapter 3); and f_{HVA} is the pulse signal used to reset the HVAs. When these block-specific clocks are not needed, the PLL can be deactivated to reduce idle power consumption.

A 480-bit shift register is loaded with front-end configuration codes and various setting bits; in terms of the latter, these bits are used to statically fix chip settings, like the clock frequencies used by the front-end blocks (SET_{CLK}) and the IDAC output current (SET_{IDAC}). In contrast, the configuration codes loaded into the shift register are dynamically multiplexed (according to the stimulator "state" encoded by 4-bit STATE bus) to the different modules of the chip, resulting in the driver being progressed through a sequence of configurations resulting in constant-current, biphasic stimulation being delivered with a stimulus timing pattern that can be adjusted on-the-fly. The key blocks and concepts of this control scheme are discussed in detail in Section 7.2.

The timing resolution for the chip-driven stimulus (e.g. pulse-width) is limited by the period of the system clock ($1/f_{CLK}$), which should be equal to the bit-width of each signal in the 4-bit STATE bus; in coming in from off-chip sources (e.g. a microcontroller), f_{CLK} and the STATE bits should also have aligned rising edges. Then, on-chip, an inverted version of f_{CLK} is used to resynchronize the front-end control signals within the "configuration decoder" block of each chip module; accordingly, there is a delay equal to $1/(2f_{CLK})$ between a stimulation protocol, encoded by STATE, entering the chip and the front-end actually executing said protocol. The chip is designed for a maximum f_{CLK} of 1MHz; to reduce idle power consumption, f_{CLK} can be set to a

lower frequency, but in doing so one must consider the resulting increase in execution delay and reduction in stimulus-pattern timing resolution.

A layout capture of the discussed bulk-CMOS stimulator chip is provided in Figure 7.2. The total chip area, including pads, is 2.64mm^2, while the active area of the chip is approximately 2mm^2.
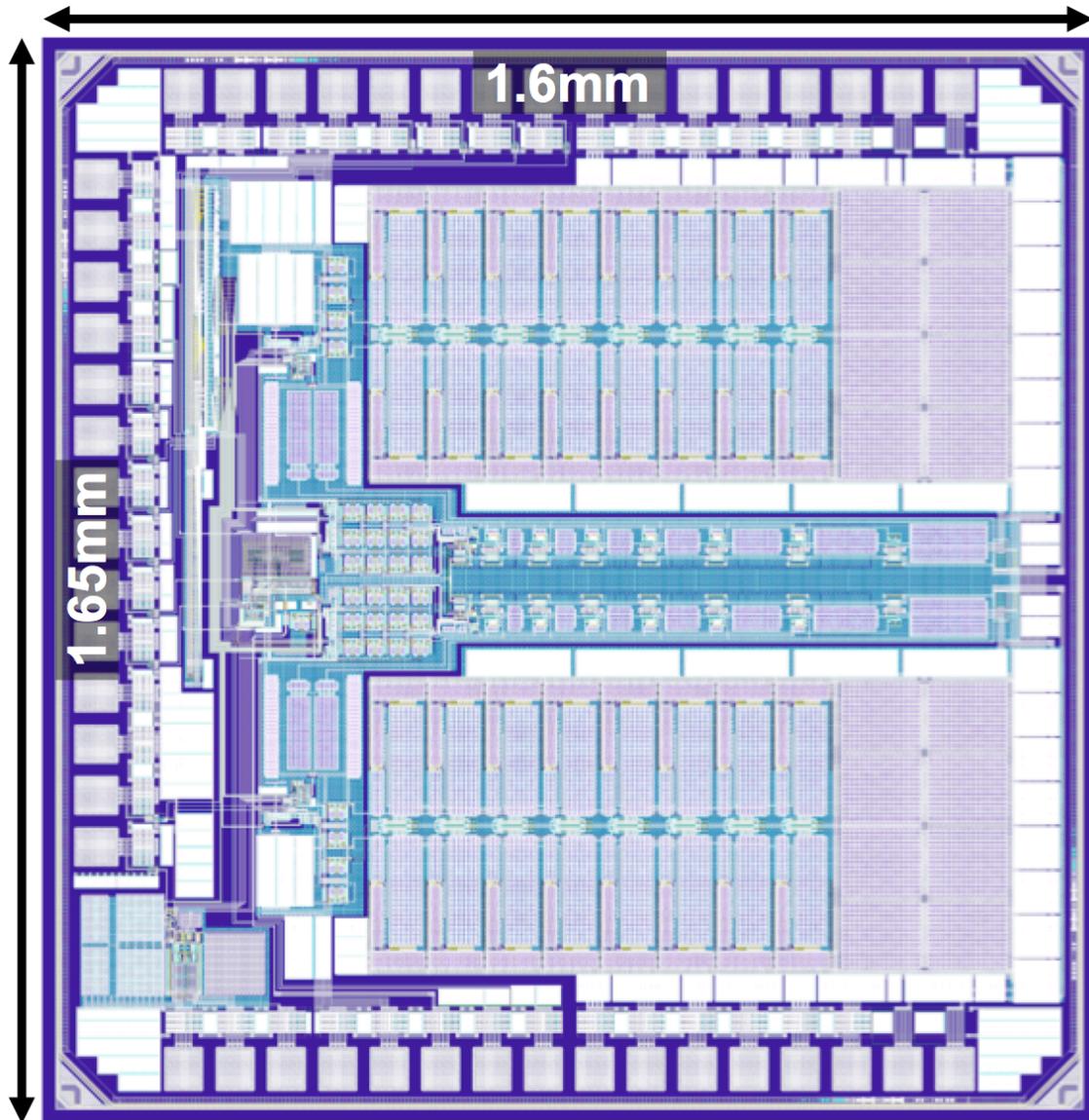
Figure 7.2. Layout capture of bulk-CMOS stimulator chip (TSMC 65nm GP CMOS).

7.2   CONTROL SUMMARY

The 4-bit, "stimulator state" encoding input (STATE) sets the overall "dynamic configuration" of the chip, and up to 12 different states can be programmed. For each chip module (0 and 1 H-bridge modules, PLL, etc.) 12 different pairs of configuration codes (1 pair for each state) are loaded into the 480-bit shift register; each pair of configuration codes consists of a primary (P) and secondary (S) set of codes. There is also an unpaired configuration code (USE P/S), which too has 12 possible values that are loaded into the shift register (1 value for each state).

Based on the A/R bit loaded into the shift register (which encodes the active/return electrode orientation) and the current value of STATE, a large digital multiplexing structure forwards the valid pairs of codes and USE P/S to the correct chip modules. The forwarded groups of configuration code pairs are $CNFG_0$, $CNFG_1$, $CNFG_{CMPX}$, and $CNFG_{PLL}$. Each $CNFG_{0(1)}$ group is composed of pairs of configuration codes for the PCD, HVA, and SW sub-systems associated with the 0(1) H-bridge module. The $CNFG_{CMPX}$ and $CNFG_{PLL}$ groups are actually just each made up of a single code pair, which encodes the enabled/disabled state of the CMP_X comparator and the PLL, respectively. Once a given configuration code pair reaches its target module, both codes contained by the pair are separately processed within a "configuration decoder" (see Figure 7.3).
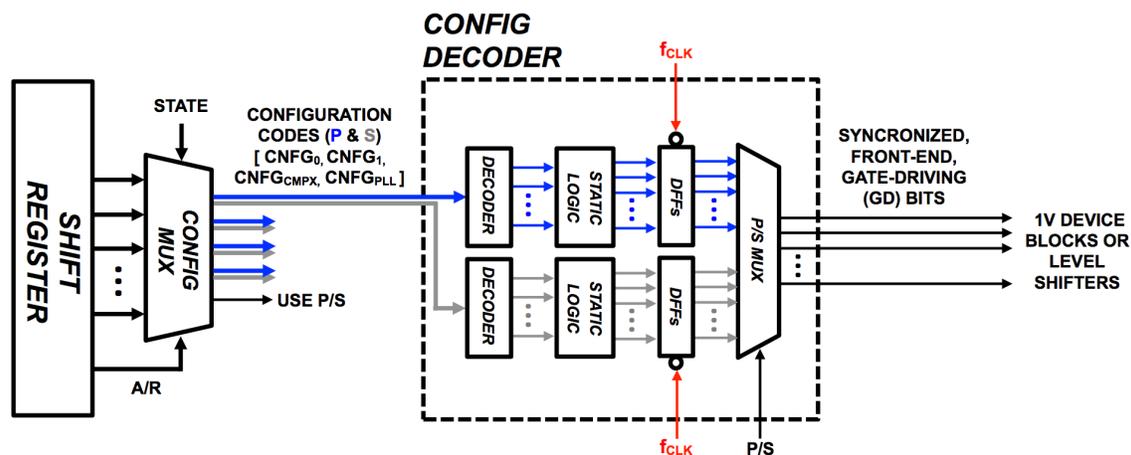
Figure 7.3. Configuration code pathway; from shift register to single-bit, gate-driving signals.

After the primary (P) code and secondary (S) code of a pair are separately decoded, module-specific static logic is used within the configuration decoder to transform the detected "configuration" (P and S) to a set of 1-bit control signals (P and S), with each signal having a dedicated gate-driving function within the "analog" portion of the module (i.e. there is no static

logic using these 1-bit control signals after leaving the configuration decoder, excluding the break-before-make logic within a low-side switch set). These gate-driving (GD) bits are then resynchronized to an inverted system clock via D-flip-flops (DFFs). After resynchronization, there are two sets of GD bits: one set corresponding to the primary (P) configuration and the other to the secondary (S) configuration of the target chip module (or module sub-system).

The P/S bit, which determines whether the primary or secondary GD signals are forwarded by a configuration decoder, is generated by the digital circuit shown in Figure 7.4; when P/S is 0, the primary configuration is active; when P/S is 1, the secondary is active. Configuration codes exist in P-S pairs to enable a fast, event-triggered change in the configuration of the stimulator front-end without having a high-frequency system clock. The event of interest is a transition at the output of CMP_X (from low to high). Accordingly, based on the configuration of the low-side switch sets, this event can be used to detect IDAC-dropout (i.e. $V_{IDAC} < V_{REF,CMPX}$) during the critical phase of stimulus delivery when balancing, constant-current stimulus is used to discharge the electrode-tissue-interface impedance (see Chapter 3), and more generally, this event can be used to detect when the voltage at the low-side of either HVA (i.e. the voltage at either electrode) falls below a low-voltage threshold (i.e. $V_{E,0} < V_{REF,CMPX}$ or $V_{E,1} < V_{REF,CMPX}$). If a given state requires this event detection, its corresponding USE P/S bit must be set to 1.
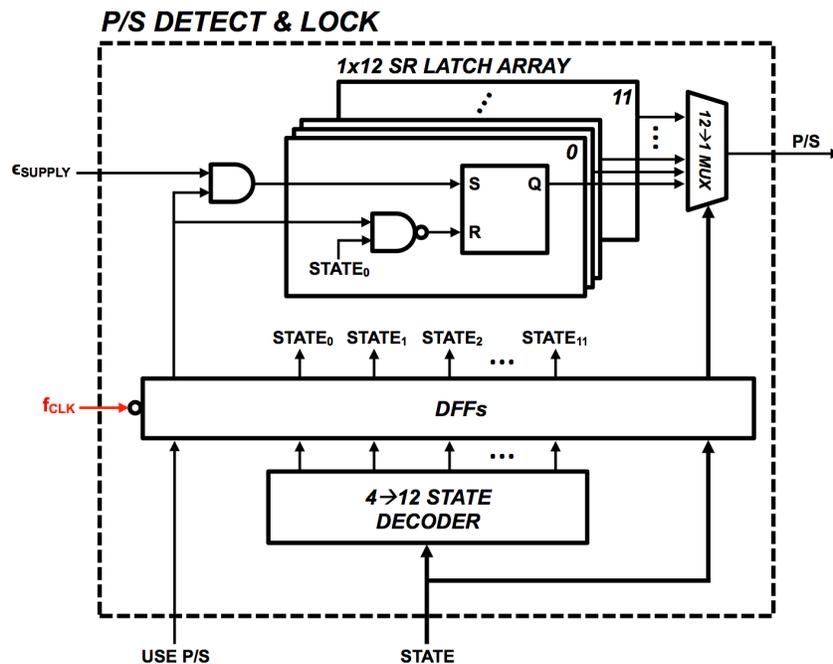
Figure 7.4. P/S configuration detecting and locking circuit.

To selectivity detect, and flag, a low-to-high transition at the output of CMP_X, and thereby force and maintain a change in the chip-wide configuration (i.e. primary to secondary), the Figure 7.4 circuit contains a dedicated SR-latch for each state (12 total latches). If the current state has been designated as requiring both primary and secondary configurations (i.e. USE P/S = 1), then the state-associated latch is enabled (i.e. R = 0), and upon a low-to-high transition at the output of CMP_X (i.e. ε_{SUPPLY}), the Q output of the latch will go to 1 and be held at such for the remaining duration of the state (regardless of any subsequent ε_{SUPPLY} transistions). If USE P/S = 0 or the current state is not associated with the index of the latch, then the R input to the latch is held at 1, keeping Q = 0. A 12-to-1 multiplier then forwards the Q corresponding to the current state to assume the role of P/S. The DFFs in Figure 7.4 are used to synchronize the described functionality with the configuration decoder blocks of the different chip modules, so that when the P/S signal arrives at said configuration decoders, the GD signals are reaching the internal multiplexer, which the P/S bit controls (Figure 7.3), at virtually the same time.

With that said, system clock (f_{CLK}) skew between the Figure 7.4 circuit and the configuration decoders of a given chip module, without any precautions taken, can potentially lead to momentary glitches in the values of the GD signals forwarded by the configuration decoders. For example, consider the stimulator transitioning between two states: "State 0" to "State 1". Assume that while in State 0, P/S was at some point set to 1, and accordingly, right before the State 0 to State 1 transition, the secondary GD signals are being forwarded by the configuration decoders. Now assume that State 1 does not have a valid secondary configuration (i.e. USE P/S = 0); accordingly, if the updated "0" value of P/S does not reach a configuration decoder by the time the new set of primary and secondary GD signals (corresponding to State 1) reach the P/S multiplexer, then the secondary GD signals of State 1 may be momentarily forwarded, even though the secondary configuration of State 1 has no meaning. Likewise, if the same occurs when State 1 does have both primary and secondary configurations (i.e. USE P/S = 1), then the secondary GD signals of State 1, which do have meaning, may be prematurely (although momentarily) forwarded.

To prevent either of these glitches from occurring, only two precautions must be made in programming the shift register with configuration codes (neither of which adversely affect the performance of the stimulator). First, for states that don't use a secondary configuration, each secondary code should be a copy of the corresponding primary code. Secondly, two consecutive

states (within the programmed state progression of the chip) must not both employ primary and secondary configurations (i.e. for one of the states USE P/S = 0).

In Appendix A tables are provided which summarize the configuration codes used by the various chip modules and module sub-systems, as well as summarize the chip "states" which are required/useful in delivering biphasic stimulus and what configuration codes each state employs. An in-depth description of the configurations of a PCD is provided in Chapter 3; the same can be found for the HVA and low-side switch set in Chapter 5.

7.3   POST-LAYOUT SIMULATIONS

To verify system functionality, the chip was simulated in driving various "high-impedance" electrode-tissue-interface impedance (Z_E) models. Excluding the PLL and the shift register, the chip was simulated using its post-layout extracted-view; to reduce simulation time, the PLL and shift register were individually verified via post-layout simulations.

Figure 7.5 provides results from one set of simulations in which the chip was programmed to deliver biphasic, constant-current stimulus with full-scale, 2mA amplitude. The pulse-width (PW) of both leading and balancing current pulses was 25μs, with a 5μs interphase delay (IPD); the short PW was used to reduce simulation time. Post-stimulus, the chip was set to allow Z_E to first passively discharge (50μs), and then forcibly discharge (50μs) via electrode shorting (although no series blocking caps were used in the simulation test bench). Following electrode shorting, the front-end of the chip was reset (i.e. capacitive dividers in PCDs and HVAs were discharged) and the chip was placed into an idle state of operation, with the PLL in its disabled, low-power configuration. To drive the full-scale 2mA stimulus, f_{DVS} for the SUPPLY PCD configuration ($f_{DVS(1)}$) was set to the maximum frequency of $f_8 = 108.48$MHz.

When using circuit simulation tools, it's convenient to use the Equation 7.1 linear approximation of the electrode-tissue-interface impedance (Z_E), derived from [3], [4], and [15] and discussed in Chapter 1.

$$Z_E \approx R_S + \left(\frac{1}{j\omega C_{DL}} \ || \ R_{CT} \right) \tag{7.1}$$

Using the Equation 7.1 approximation, the values of Z_E used in the Figure 7.5 simulations were chosen to force the chip to approach its ±11V compliance limit during stimulus delivery, with each of the four evaluated models having different "high impedance" combinations of the

spreading resistance (R_S), double-layer capacitance (C_{DL}), and charge-transfer resistance (R_{CT}), including combinations resulting in purely resistive and purely capacitive Z_E impedances.
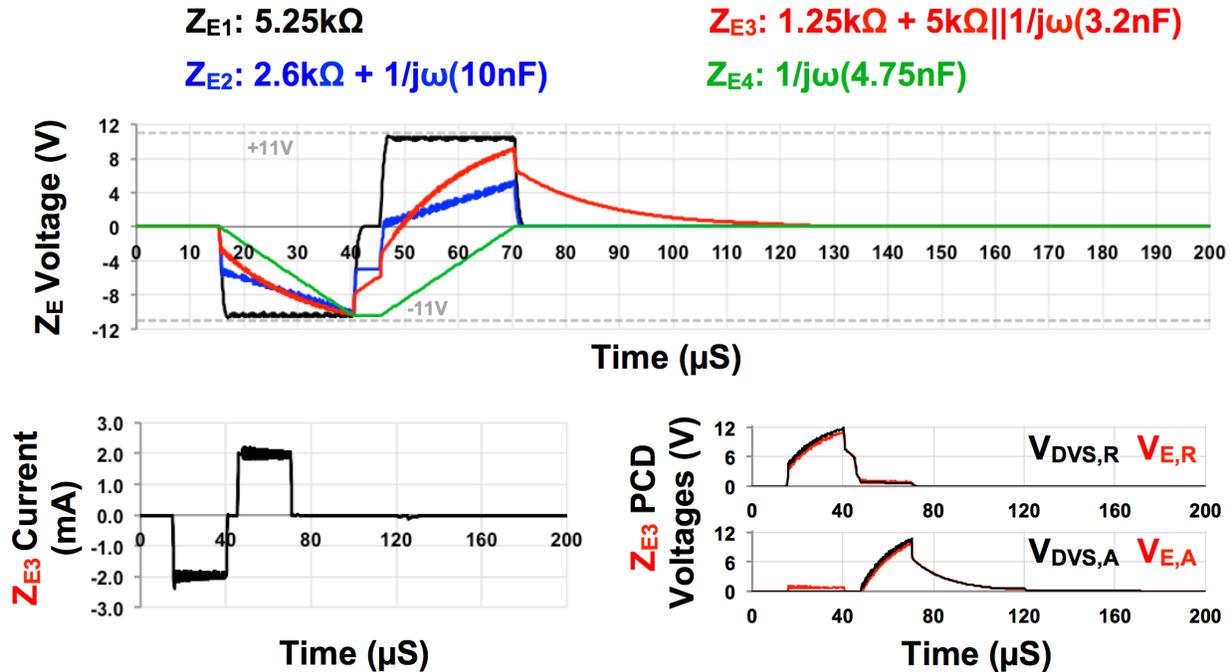
Figure 7.5. 2mA biphasic stimulation simulations; 25µs PW, 5µs IPD, stimulus followed by passive and forced discharge (in said order), and no series blocking capacitors; f_{CLK} = 1MHz, LVDD/VDD = 1V/2.5V, $f_{DVS(1)}$ = $f_{DVS(SUPPLY)}$ = f_8.

The waveforms in the top-half of Figure 7.5 show the voltage across Z_E, for each of the four evaluated Z_E models, during simulated stimulus delivery. Accordingly, the percentage of the balancing-pulse duration that the voltage across Z_E is positive depends on the capacitive/resistive nature of Z_E; i.e. when the Z_E voltage is negative during balancing-pulse delivery, the PCD associated with the active electrode is not being employed and the stimulation current is instead supplied by Z_E, which is being discharged.

The waveforms in the bottom-half of Figure 7.5 show the stimulus current (referenced to the active electrode) and the PCD voltages associated with Z_{E3} stimulation. The stimulus current, while having a ripple due to the switched-capacitor operation and ON/OFF regulation of the DVSs, still appears as a well-regulated constant-current biphasic waveform. Furthermore, the observed balancing-pulse shape demonstrates the two sub-phases of balancing-stimulus delivery

(i.e. the ripple due to the active DVS doesn't appear until a few microseconds after balancing-pulse delivery has begun, since Z_E is first discharged via the stimulus current).

The PCD voltages in Figure 7.5 demonstrate the on-demand voltage generation on each side of the H-bridge front-end, as well as the operation of the PCDs in the SUPPLY and TRACK feedback configurations (discussed in Chapter 3).

Table 7.1 provides relevant chip performance metrics measured during the Figure 7.5 simulations. The data in Table 7.1 demonstrates that regardless of the capacitive/resistive nature of Z_E, the stimulator design, at full-scale stimulus, closely regulates the average amplitude of both current pulses (leading and balancing) to the nominal value (2mA); the ripple voltages/current seen in Figure 7.5 are accordingly an "invisible" high-frequency AC artifact of the delivered stimulus.

Table 7.1. Performance Metrics from Figure 7.5 Simulations

Z_E	I_{AVE} (NEG) Delivered (mA)	I_{AVE} (POS) Delivered (mA)	I_{DC} Delivered @ 1kHz (nA)**	P_{AVE} (NEG) Consumed (mW)	P_{AVE} (POS) Consumed (mW)	P_{AVE} Consumed @ 1kHz (mW)	P_{AVE} Consumed @ IDLE (μW)
1	-1.957	1.959	60.4*	60.3	50.96	51.06	2.82	
2	-1.974	1.967	106.7*	8.4	48.38	45.61	2.62	210***
3	-1.980	1.980	93.7*	-513.3	48.71	43.38	2.57	
4	-1.981	1.989	290.0*	22.2	48.31	5.27	1.60	

*Evaluated before forced discharge

**No blocking capacitors used in-series with Z_E

*** 1MHz system clock

Table 7.1 also shows the residual DC current for the delivered full-scale 2mA stimulus, evaluated at an unrealistically high 1kHz stimulation rate, is on the order of 100nA (if only passive discharge is employed post-stimulus) for the different Z_E test cases. With that said, DC currents on the order of 1nA could be realized if large capacitors were to be included in-series with the electrodes (see 8.4nA residual current result for Z_{E2}, which has a series capacitance, with no parallel R, in its electrode model).

The efficiency of the stimulator front-end chip, while delivering maximum output power, is also demonstrated by the Table 7.1 data. While stimulating the resistive Z_{E1} impedance, an average input power of approximately 51mW was observed during the delivery of each pulse

(which includes all bias currents to the chip). The average power delivered to Z_E during each phase of the stimulus can be estimated as 21.2mW (i.e. 2mA at 10.6V). Accordingly, the simulated stimulator efficiency, while delivering maximum output power, is approximately 41%. However, the input power of the DVS circuits, which dominate chip power consumption, is relatively constant for a given load current across the output voltage range. Accordingly, if the chip were used to drive 2mA stimulus through a lower-impedance Z_E, the power consumed by the chip would not decrease proportionally with the reduction in delivered power to Z_E, resulting in a drop in efficiency from the 41% figure (this is undoubtedly a drawback of this front-end design, as is). Table 7.1 also shows that while the average power consumed during leading-pulse delivery is relatively constant, regardless of Z_E, the power consumed during balancing-pulse delivery is highly dependent on Z_E, due to the C_{DL} of Z_E supplying the stimulus current (instead of a SUPPLY-configured PCD) as long as the voltage across Z_E (i.e. $V_{E,A} - V_{E,R}$) remains negative.

The average power consumption of the chip depends not only on the power consumed in delivering each pulse, but also the employed stimulation protocol (e.g. PW, stimulus frequency, etc.). Table 7.1 provides an estimation of the average power that would be consumed by the chip if the Figure 7.5 stimulus event, for each Z_E impedance, were to be carried out at an unrealistically high rate of 1kHz. Accordingly, with a 1ms interval between the beginning of consecutive stimulation events, the stimulator would be in the idle, low-power configuration most of the time, bringing the average chip power consumption, for full-scale 2mA stimulation with 25µs PW, to levels below 3mW. The idle power consumption of the chip was observed to be approximately 210µW; the primary contributors to this figure are the DC bias currents used by the PLL and IDAC (even when disabled), 1MHz system clocking, and leakage currents in the 1V, thin-oxide devices.

Similar simulations were performed, but with 50µA stimulus amplitude, as to demonstrate the chip operating at the low-end of its stimulus range. The timing parameters of the driven stimulus were programmed to be the same as with the full-scale 2mA simulations, and like with the full-scale simulations, values for Z_E were chosen (each having a different combination of R_S, C_{DL}, and R_{CT}) to force the chip to operate near its compliance limit (±11V). Figure 7.6 shows the observed stimulation voltage/current waveforms from these simulations, and the corresponding chip performance is given in Table 7.2.

Figure 7.6. 50µA biphasic stimulation simulations; 25µs PW, 5µs IPD, stimulus followed by passive and forced discharge (in said order), and no series blocking capacitors; f_{CLK} = 1MHz, LVDD/VDD = 1V/2.5V, $f_{DVS(1)}$ = $f_{DVS(SUPPLY)}$ = f_1.

Table 7.2. Performance Metrics from Figure 7.6 Simulations

Z_E	I_{AVE} (NEG) Delivered (µA)	I_{AVE} (POS) Delivered (µA)	I_{DC} Delivered @ 1kHz (nA)**	P_{AVE} (NEG) Consumed (mW)	P_{AVE} (POS) Consumed (mW)	P_{AVE} Consumed @ 1kHz (mW)	P_{AVE} Consumed @ Idle (µW)
1	-45.23	45.26	2.5* | 2.4	4.37	4.65	0.54	
2	-47.66	47.82	-12.9* | 0.3	4.19	3.09	0.50	210***
3	-49.17	49.54	-2.4* | -16.5	4.30	4.15	0.51	
4	-49.37	46.68	24.6* | 3.3	4.16	0.50	0.45	

*Evaluated before forced discharge

**No blocking capacitors used in-series with Z_E

*** 1MHz system clock

In comparing Figure 7.6 and Figure 7.5, there are visible differences in the voltage and current ripple amplitudes. The larger amplitude observed in the Figure 7.6 simulations is due to 50µA being significantly less than the current the DVS supplies in a $f_{DVS(1)}$ = $f_{DVS(SUPPLY)}$ = f_1 clock cycle; additionally, when a PCD is in the SUPPLY configuration, the additional

$f_{DVS(SUPPLY)}$ pulses the DVS is forwarded due to the PCD loop delay further amplifies said ripple amplitude.

Accordingly, the observed ripple amplitude during 50μA stimulus delivery could be potentially reduced if a clock frequency lower than 13.56MHz were set as $f_{DVS(SUPPLY)}$; likewise, since the ripple amplitude is what actually limits the low-end of the stimulation current range to 50μA, if $f_{DVS(SUPPLY)}$ could be set to be lower than 13.56MHz (e.g. 13.56MHz/2, 13.56MHz/4, etc.) the chip could be potentially used to stimulate with current as low as 10μA (i.e. the lowest setting of the on-chip IDAC).

But even with the observed ripple, Table 7.2 shows that across the evaluated Z_E impedances, the chip regulates the average stimulus current in each pulse to be within 10% of the nominal. For Z_{E1} and Z_{E2}, leading and balancing pulses are regulated to approximately the same level; for these two impedances, the average is significantly less than the nominal because the sub-nominal current delivered within the rise-time interval of each pulse is included in the evaluation of the average. The relatively large difference between the leading and balancing average currents for Z_{E4} can be jointly attributed to parasitic capacitances in the stimulus current path and the asymmetric operation of the H-bridge front-end when driving a purely capacitive Z_E.

Table 7.2 also shows that the discussed variation and mismatch in leading/balancing average current doesn't seem to significantly impact the resulting DC residual current (evaluated at a high 1kHz stimulus rate), which is on the order of 10nA (via passive or forced discharge) for the different evaluated Z_E models. As with the full-scale stimulus simulations, the residual DC current could be further reduced if series blocking capacitors were to be employed (see Z_{E2} in Table 7.2). In terms of the average power consumption, Table 7.2 shows the same trends as observed in Table 7.1, but with lower magnitudes (except for the idle power consumption figure, which remains fixed at 210μW).

7.4   PRELIMINARY STATE-OF-THE-ART COMPARISON

Table 7.3 provides a comparison between the described high-voltage neural stimulator chip and other bulk-CMOS stimulator systems that employ front-ends demonstrating compliance levels greater than the VDD-rating of the devices each were implemented with.

Table 7.3. State-of-the-Art Comparison Table

System	[11] T. BioCAS '13*	[12] JSSC '15	[13] JSSC '14	This Work (Post-Layout Simulations)
Driver Topology	Ground Return	Differential	H-bridge	H-bridge
Process	65nm CMOS (TMSC LP)	65nm CMOS (TSMC LP)	0.18μm CMOS (TSMC)	65nm CMOS (TSMC GP)
Devices Used / Voltage Compliance	1.2V, 2.5V / ±2.4V	1.2V, 2.5V / ≈ ±6V	1.8V, 3.3V / ≈ ±9V	1V, 2.5V / ≈ ±11V
Electrode Invariant	R→Yes, C→Yes	C→Yes, R→?	R→Yes, C→No	R→Yes, C→Yes
Charge-Balancing Technique	Digital Calibration	Electrode Shorting	N.A.	Electrode Shorting
Min I_{STIM} / Max I_{STIM} / IDAC	N.A. / 50μA / 4-bit, ≈ 3μA LSB	N.A. / 450μA** / 6-bit, 7μA LSB	30μA / 30μA / 1-bit	50μA / 2mA / 8-bit, 10μA LSB
# Electrode Pads / # Stimulators	513 / 512	8 / 2	2 / 1	2 / 1
Active Area	0.0169mm^2 /stimulator	0.385mm^2 + 0.0675mm^2 /stimulator	≈ 1mm^2	2mm^2
Efficiency @ Max Output Power — DC-DC	76%	62%	43-72%	50%
Efficiency @ Max Output Power — Stimulator*	≈ 20%*****	< 62%****	N.A.	41%****

*Can generate "arbitrary" stimulus waveforms; other systems are constant-current only

**Demonstrated up to 150μA

***Evaluated while delivering maximum biphasic I_{STIM} to real Z_E at maximum electrode voltage

****Single stimulator, rectification and voltage regulation prior to HVDD generation (via DC-DC) NOT considered

*****Full system stimulating with 10% stimulus duty cycle at 50% activity factor (consumes 15mW)

For fair and normalized comparisons, Table 7.3 only focuses on system performance relevant to the front-end stimulation electronics, since the referenced works feature highly integrated systems in which the stimulator is one of several functional blocks implemented in CMOS (e.g. may also include integrated neural recording, wireless interfaces, etc.). Additionally,

the performance figures provided for this work have been obtained through post-layout, extracted-view simulations, while the performance of [11], [12], and [13] have at least been partially verified with chip measurements.

7.4.1 *Voltage Compliance, Stimulation Current, and Electrode-Invariance*

Measurements pending, Table 7.3 shows that for applications requiring a low number of stimulation electrodes, this work may be the best suited, among the current state-of-the-art, for general-use applicability, demonstrating the highest voltage compliance, largest maximum stimulus current, and widest stimulus current range. Additionally, as compared to [12] and [13] (the two most similar works in terms of performance and topology), this work shows to be the most "electrode-invariant", demonstrating the ability to reliably deliver biphasic, constant-current stimulus to a wide range of Z_E impedances, from purely resistive to purely capacitive, low-impedance to high-impedance.

7.4.2 *Efficiency*

The overall efficiency of this work, at both high and low stimulation voltages, is comparable to [13], considering that [13] employs a standard H-bridge topology and has a DC-DC converter with efficiency similar to the DVS used in this work. However, the stimulator efficiency of [12] surpasses the presented work, most so at low stimulation voltages, since 1) the effective efficiency of its DC-DC converter is made to be relatively constant across the stimulation voltage range of the system by utilizing a high-voltage switching network to multiplex the voltage taps of its DC-DC converter, as to provide quasi "adiabatic" voltage rails for its differential front-end, and 2) the configuration of the DC-DC converter enables charge-recycling during balancing-pulse delivery (if Z_E looks capacitive). In the future, the former of these efficiency-boosting mechanisms could be potentially applied to the presented work.

The peak efficiency of the DVS is less than that of the DC-DC converters featured in [12] and [13] primarily because the DC power input of the DVS is chip ground instead of VDD, which is done to enable 0V to 12V generation at the DVS output. However, as consolation for this reduced efficiency, the DC power rails (VDD and LVDD) of the presented work are essentially capacitively isolated from the electrode terminals (as if large series blocking

capacitors were used in the stimulation current path), making this work intrinsically safer and more fault-proof than [11], [12], and [13].

7.4.3 *Electrode Pads and Stimulators On-Chip*

A potential shortcoming of this work, compared to the state-of-the-art, is the number of electrodes the stimulator chip can directly interface with, as well as the number of stimulators on-chip. Like [13], this work features a single on-chip stimulator front-end that interfaces with two pads, with each pad associated with a single electrode. Unlike differential or ground-return stimulators, two (or more) H-bridge-style stimulators cannot be reliably used to simultaneous drive balanced, biphasic stimulus through different active/return electrode pairs. Fortunately, this does not prohibitively limit the potential uses of an H-bridge-style stimulator, since many neural stimulation applications, while perhaps requiring the stimulator to interface with more than two electrodes, do not require stimulus delivery through more than two electrodes (active and return) at the same time. Accordingly, an off-chip analog demultiplexer, implemented with high-voltage-tolerant switches, can be used to interface the presented chip with any number of electrodes demanded by a given stimulation application; on-chip demultiplexing to more than two electrode pads, with only a single stimulator on-chip, would require high-voltage-tolerant, analog switch structures implemented in a low-voltage bulk-CMOS process (which presents serious integration challenges).

In future work, it may be possible to enable on-chip electrode demultiplexing by integrating more than two H-bridge modules on the same die, with only a few modifications in the module design compared to what is used in this work (see Section 7.1). Accordingly, if a system had four of said H-bridge modules, each interfacing with a dedicated electrode pad, biphasic constant-current could be delivered between any two electrode pads, in either polarity (active/return, return/active).

7.4.4 *Form-Factor*

Table 7.3 suggests that another potential drawback of the presented system is its form-factor, which, in terms of area/stimulator, exceeds [11], [12], and [13]. The small form-factor demonstrated by [11] is achieved through the 512 on-chip stimulators (each employing the ground-return topology and accordingly, interfacing with a dedicated active electrode and

sharing a common return electrode) being powered by a common, single-stage DC-DC converter which generates HVDD = 2VDD, with the exact area of said converter being small (i.e. < $0.1mm^2$) but not explicitly disclosed (and therefore not included in the Table 7.3 active area estimate). This small single-stimulator area comes at the cost of limited performance, with the ±2.4V compliance of [11] insufficient for many neural stimulation applications, including potentially epiretinal stimulus, for which the system is design for (i.e. other demonstrated epiretinal stimulation systems are implemented in high-voltage technologies to achieve requisite compliance levels [7]).

To generate an HVDD that is significantly greater than 2VDD, the stimulation systems in [12] and [13] each employ a multi-stage DC-DC converter, based on switched-capacitor operation and requiring a large chip area. Accordingly, [12] and [13] share more similarities with the presented system than [11] does. The stimulator demonstrated in [13] is approximately 2x smaller than the presented work, in terms of active area. However, considering that, compared to [13], the presented system has both higher voltage compliance (approximately 1.2x) and higher maximum stimulus current (approximately 66x), it can be argued the presented system, in demonstrating approximately 40x higher maximum-stimulus-power/stimulator-area, is significantly more "area-efficient" than [13]. Considering this same area-efficiency metric, [12] and this work "perform" approximately the same, if for [12] the "stimulator-area" is evaluated as the total area of the stimulation system (DC-DC converter and two stimulators) divided by two; if instead the "stimulator-area" is evaluated the area of the DC-DC converter and one stimulator, than the presented work is approximately 1.8x more area-efficient than [12].

7.4.5 *Idle Power Consumption*

The idle, or stand-by, power draw is a critical performance metric for a potentially implantable neural stimulator, since for most of the time a stimulation system may not be delivering stimulus. This metric is not included in Table 7.3 because said performance was not provided in [11] and [12]. However, the idle power draw observed for this work in the Section 7.3 simulations (210µW with a 1MHz system clock) is comparable to [13] (165µW). The idle power draw for the presented work could easily be made lower by reducing the system clock frequency, and in future versions of this system, the idle draw could be further reduced by: 1) using less leakage-

prone low-voltage devices; 2) implementing the frequency synthesis block as an all-digital PLL (ADPLL); and 3) using fully-dynamic comparators.

Chapter 8. CONCLUSION

A new neural stimulator front-end design is presented which can achieve high-voltage compliance while being safely implemented using low-voltage, bulk-CMOS devices. The front-end employs a modified H-bridge topology to operate with invariance to the resistive/capacitive nature of the electrode-tissue-interface impedance (Z_E). Additionally, the specialized circuit blocks within the front-end allow the bipolar voltage compliance, in driving biphasic constant-current stimulus, to be set to an arbitrarily high-level, only limited by the breakdown voltages of metal-to-metal capacitor structures and parasitic junctions within a given integrated process.

The two specialized circuits that enable the proposed front-end functionality are the dynamic voltage supply (DVS) and high-voltage adapter (HVA). These circuits are presented at the transistor-level, and mathematical modeling expressions and implementation considerations pertaining to said circuits are also provided. Furthermore, to demonstrate the unique functionality of both circuits, post-layout simulation results are provided, and measurement results for a fabricated DVS circuit (in 65nm bulk-CMOS) are presented and discussed.

To verify the efficacy of an H-bridge-based stimulation system (like the proposed integrated front-end) in real-world neural stimulation applications, a PCB-based prototype has been designed, built, and used in *in-vivo* (rat) experiments. Aside from verifying the stimulus regulating ability of an H-bridge-based stimulator, the presented results from said experiments show the proposed integrated topology, if implemented in a modern bulk-CMOS technology, should have sufficient voltage compliance for neural stimulation applications relevant to the development of bidirectional brain-computer interfaces (BBCIs), such as subdural-cortical, intramuscular, and intraspinal stimulation.

The design of a 65nm bulk-CMOS chip that features the full implementation of the proposed front-end system is also presented and discussed. Post-layout simulations of the integrated stimulator demonstrate approximately ±11V compliance across the 50μA to 2mA stimulus amplitude range that can be driven by the chip. This stimulus driving ability and a demonstrated invariance to the resistive/capacitive characteristics of the electrode-tissue-interface impedance suggest that, measurements pending, this chip compares favorably with the state-of-the-art while advancing the voltage-compliance, current-driving ability, and general-use applicability that can be achieved by a low-voltage, bulk-CMOS stimulation system.

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APPENDIX A: STIMULATOR CHIP CONTROL TABLES

Table A.1. Positive-Current Driver (PCD) Configuration Code Summary

Configuration #	Configuration Description	Code		
		B2	B1	B0
0	IDLE	0	0	0
1	SUPPLY	0	0	1
2	TRACK	0	1	0
3	BLEED DOWN	0	1	1
4	DISCHARGE, RESET	1	0	0
5	UNASSIGNED	1	0	1
6	UNASSIGNED	1	1	0
7	UNASSIGNED	1	1	1

Table A.2. CMP_X Configuration Code Summary

Configuration #	Configuration Description	Code
		B0
0	OFF, DISABLED	0
1	ON, ENABLED	1

Table A.3. PLL Configuration Code Summary

Configuration #	Configuration Description	Code
		B0
0	OFF, DISABLED	0
1	ON, ENABLED	1

Table A.4. High-Voltage Adapter (HVA) Configuration Code Summary

Configuration #	Configuration Description	Code	
		B1	B0
0	OFF	0	0
1	IDLE	0	1
2	ACTIVE	1	0
3	RESET	1	1

Table A.5. Low-Side Switch Set (SW) Configuration Code Summary

Configuration #	Configuration Description	Code		
		B2	B1	B0
0	HIGH Z	0	0	0
1	GND VIA SHRT	0	0	1
2	GND VIA Z	0	1	0
3	CMP ONLY	0	1	1
4	CMP, IDAC	1	0	0
5	CMP, GND VIA SHRT	1	0	1
6	CMP, GND VIA Z	1	1	0
7	UNASSIGNED	1	1	1

Table A.6. Stimulator Chip State Summary

State Info							Active-Side Configurations (#)			Return-Side Configurations (#)			CMP$_X$ CNFG #	PLL CNFG #	USE P/S
#	State Bits				Description	P/S	PCD	HVA	SW	PCD	HVA	SW			
	B3	B2	B1	B0											
0	0	0	0	0	IDLE W/O PLL	P	0	1	1	0	1	1	0	0	0
						S	0	1	1	0	1	1	0	0	
1	0	0	0	1	IDLE W/ PLL	P	0	1	1	0	1	1	0	1	0
						S	0	1	1	0	1	1	0	1	
2	0	0	1	0	ACTIVE ELECT. NEG STIMULUS	P	0	1	4	1	2	0	1	1	0
						S	0	1	4	1	2	0	1	1	
3	0	0	1	1	INTERPHASE DELAY	P	0	1	1	2	2	3	1	1	0
						S	0	1	1	2	2	3	1	1	
4	0	1	0	0	ACTIVE ELECT. POS STIMULUS	P	0	1	1	2	2	4	1	1	1
						S	1	2	0	3	2	4	1	1	
5	0	1	0	1	UNMONITORED PASSIVE DISCHARGE	P	2	2	3	2	2	1	1	1	0
						S	2	2	3	2	2	1	1	1	
6	0	1	1	0	UNMONITORED FORCED DISCHARGE	P	2	2	6	3	2	1	1	1	0
						S	2	2	6	3	2	1	1	1	
7	0	1	1	1	DVS RESET	P	4	1	1	4	1	1	0	1	0
						S	4	1	1	4	1	1	0	1	
8	1	0	0	0	HVA RESET	P	0	3	1	0	3	1	0	1	0
						S	0	3	1	0	3	1	0	1	
9	1	0	0	1	MONITORED PASSIVE DISCHARGE	P	2	2	3	3	2	1	1	1	1
						S	3	2	3	3	2	1	0	1	
10	1	0	1	0	MONITORED FORCED DISCHARGE	P	2	2	5	3	2	1	1	1	1
						S	3	2	5	3	2	1	0	1	
11	1	0	1	1	UNASSIGNED	P	0	0	0	0	0	0	0	0	0
						S	0	0	0	0	0	0	0	0	

APPENDIX B: DERIVATION OF DVS CIRCUIT APPROXIMATE STEADY-STATE MODEL

This appendix covers the derivation of expressions that can be used to estimate the steady-state performance of a constant-current loaded, multi-stage voltage-doubler circuit; specifically, a voltage-doubler circuit of the DVS topology presented in Chapter 4.

Figure B.1 can be used to represent the functionality of a single-stage DVS circuit in its SOURCE setting. This operational model has four phases; $C_{PAR,TP}$ and $C_{PAR,BP}$ are the lumped top-plate and bottom-plate parasitic capacitance, respectively, observed during SOURCE-setting operation.
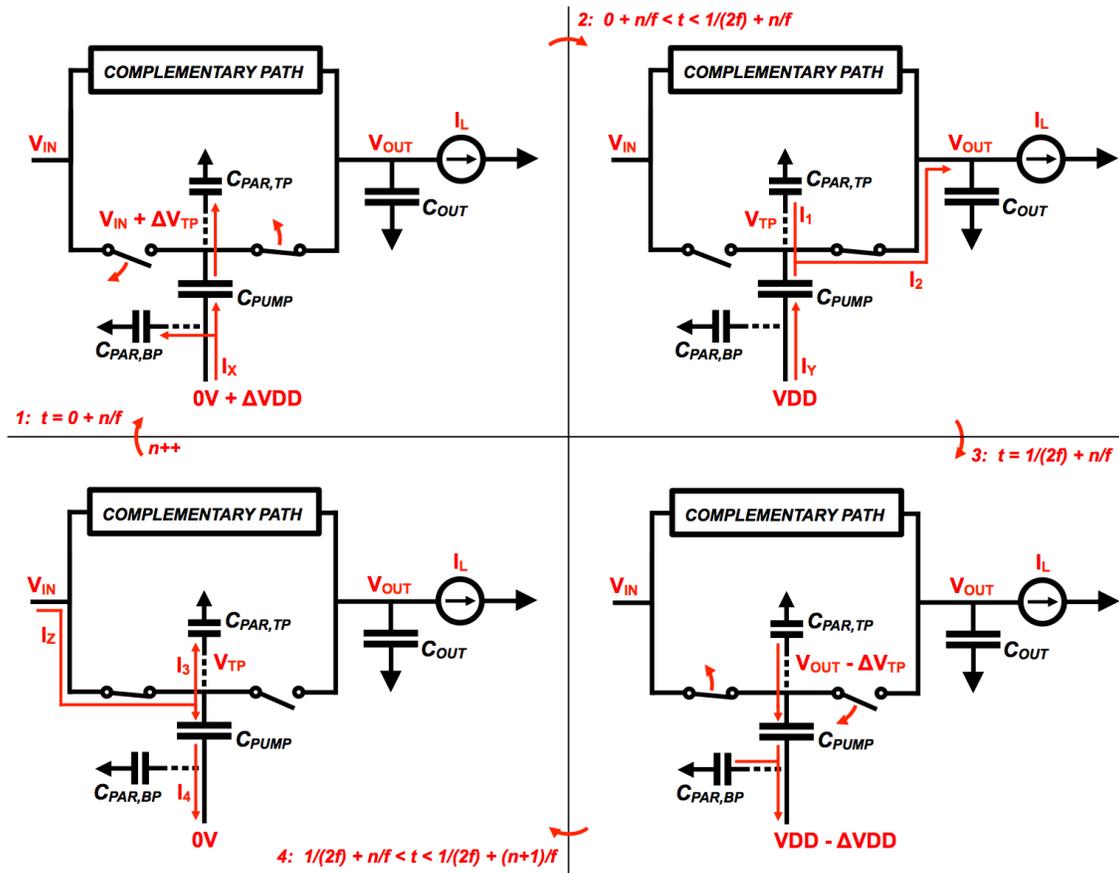

Figure B.1. Improved model of DVS/voltage-doubler operation; $C_{PAR,BP}$ and $C_{PAR,TP}$ are lumped parasitic capacitances, ΔV_{TP} is attenuated version of ΔVDD (determined by C_{PUMP}, $C_{PAR,TP}$ capacitive divider); the signal applied to the bottom-plate of C_{PUMP} is a 50% duty-cycle, 0V to VDD pulse signal, with instantaneous rise/fall-time and frequency f; $V_{IN} \leq V_{OUT}$.

Efficiency (ε) for a charge-supplying power-converter will be defined as the average output power (P_{OUT}) divided by the average input power (P_{IN}). With regards to Figure B.1, P_{OUT} is $I_L \times V_{OUT}$ (average) and P_{IN} is defined by Equation B.1. $I_{X,AVE}$, $I_{Y,AVE}$, and $I_{Z,AVE}$ are I_X, I_Y, and I_Z, respectively, integrated over the duration of the corresponding phase (of Figure B.1 operation) in which each appears, and averaged over the duration of an entire switching period (i.e. 1/f); the "2" coefficient in Equation B.1 is required since there are two complementary paths, and said currents only apply to the operation of one path.

$$P_{IN} = 2\left(I_{X,AVE}VDD + I_{Y,AVE}VDD + I_{Z,AVE}V_{IN}\right) \tag{B.1}$$

I_L (the constant-current load) and VDD are known quantities, so only expressions for $I_{X,AVE}$, $I_{Y,AVE}$, $I_{Z,AVE}$, and V_{OUT} must be found in order to obtain an expression for ε. In deriving said expressions, it is assumed that the switches in Figure B.1 behave ideally, exhibiting negligibly small switching resistance and allowing complete charge-transfer (virtually) whenever closed. It is also assumed that steady-state operation has been reached (i.e. the average switched-capacitor current supplied by the circuit matches I_L) and $C_{OUT} \gg C_{PUMP}$; these assumptions allow V_{OUT} to be treated as a DC voltage. Lastly, the rise-time and fall-time of the pulse signal applied to the bottom-plate of C_{PUMP} are assumed to be instantaneous.

Considering the Figure B.1 cycle, before ΔVDD is applied to the bottom plate of C_{PUMP}, the top-plate of C_{PUMP} is charged to V_{IN}, with the bottom-plate grounded. Then, at t = 0 + n/f (phase-one), a 0V to VDD transition occurs at the bottom-plate of C_{PUMP}, simultaneously charging $C_{PAR,BP}$ to VDD. Since the rise-time of the voltage shift is assumed instantaneous, $C_{PAR,TP}$ experiences a voltage change of ΔV_{TP}, where ΔV_{TP} is determined by the ratio of the capacitive divider formed by $C_{PAR,TP}$ and C_{PUMP} (see Equation B.2).

$$\Delta V_{TP} = VDD \left(\frac{C_{PUMP}}{C_{PUMP} + C_{PAR,TP}}\right) \tag{B.2}$$

Although not shown in Figure B.1, an inverter is driving the bottom-plate of C_{PUMP}, and therefore the source of I_X, which charges the two parasitic capacitances during this phase, is VDD (see the definition of the $I_{X,AVE}$ contribution to P_{IN} in Equation B.1); this parasitic charging occurs once every switching cycle. To find $I_{X,AVE}$, the charge required to produce the said voltage changes across $C_{PAR,BP}$ and $C_{PAR,TP}$ can be divided by the switching period (1/f), giving Equation B.3.

$$I_{X,AVE} = \left[C_{PAR,BP}VDD + \left(\frac{C_{PUMP}C_{PAR,TP}}{C_{PUMP} + C_{PAR,TP}} \right)VDD \right]f \tag{B.3}$$

Once t > 0 + n/f, charge-sharing between the in-parallel C_{PUMP} + $C_{PAR,TP}$ network and C_{OUT} begins, with the top-plate voltages of these three capacitors equalizing before phase-two is over (since the switching resistance is assumed to be negligibly small compared to the switching period). This charge-sharing will reduce the voltage at the top-plates of C_{PUMP} and $C_{PAR,TP}$ by ΔV_Y.

$$\Delta V_Y = V_{TP}\left(0^+ + \frac{n}{f} \right) - V_{TP}\left(\frac{1}{2f}^- + \frac{n}{f} \right) = V_{IN} + \Delta V_{TP} - V_{OUT} \tag{B.4}$$

The charge transferred to C_{OUT} within the phase-two time interval (via current I_2) should offset the draw from the constant current load I_L. Accordingly, Equation B.5 relates ΔV_Y to I_L and the switching frequency f.

$$I_L = \frac{1}{\left(\frac{1}{2f}\right)} \int_{0^+ + \frac{n}{f}}^{\frac{1}{2f}^- + \frac{n}{f}} I_2(t)dt = \Delta V_Y \left(C_{PUMP} + C_{PAR,TP} \right)2f \tag{B.5}$$

Solving Equation B.5 for ΔV_Y,

$$\Delta V_Y = \frac{I_L}{2f\left(C_{PUMP} + C_{PAR,TP} \right)} \tag{B.6}$$

During said charge sharing, C_{PUMP} and $C_{PAR,TP}$ each contribute to the I_L offsetting current I_2 (via I_Y and I_1, respectively), and the division of these currents is simply determined by the ratio of the two capacitances. Therefore, considering Equation B.5, which relates I_L to I_2 integrated over half a switching period, the current delivered by VDD to the bottom plate of C_{PUMP} during phase-two, averaged over one complete switching period ($I_{Y,AVE}$) is given by Equation B.7.

$$I_{Y,AVE} = \frac{1}{\left(\frac{1}{f}\right)} \int_{0^+ + \frac{n}{f}}^{\frac{1}{2f}^- + \frac{n}{f}} \left(\frac{C_{PUMP}}{C_{PUMP} + C_{PAR,TP}} \right)I_2(t)dt = \left(\frac{C_{PUMP}}{C_{PUMP} + C_{PAR,TP}} \right)\frac{I_L}{2} \tag{B.7}$$

At t = 1/(2f) + n/f (phase-three), the falling pulse edge drives the bottom-plate of C_{PUMP} back down to 0V, and the switches connected to the top-plate of C_{PUMP} reverse their open/closed configurations. This instantaneous bottom-plate negative voltage shift of $-\Delta VDD$ results in a top-plate negative voltage shift with the same magnitude as Equation B.2 (i.e. $-\Delta V_{TP}$); the charge removed from parasitic capacitance during this phase returns to ground.

Once t > 1/(2f) + n/f, V_{IN} begins recharging C_{PUMP} and $C_{PAR,TP}$ (phase-four). Considering Equation B.4 and the $-\Delta V_{TP}$ observed at the C_{PUMP} top-plate node in phase-three, the voltage change across C_{PUMP} and $C_{PAR,TP}$ due to the "recharge" current I_Z (Equation B.8) must satisfy Equation B.9.

$$\Delta V_Z = V_{TP}\left(0^- + \frac{n+1}{f}\right) - V_{TP}\left(\frac{1}{2f}^+ + \frac{n}{f}\right) \tag{B.8}$$

$$0 = \Delta V_{TP} - \Delta V_Y - \Delta V_{TP} + \Delta V_Z \tag{B.9}$$

Therefore,

$$\Delta V_Z = \Delta V_Y \tag{B.10}$$

Accordingly, the total charge delivered to C_{PUMP} and $C_{PAR,TP}$ during phase-four (via I_Z) is equal to the total charge removed from these same capacitors during phase-two. Therefore,

$$I_{Z,AVE} = \frac{1}{\left(\frac{1}{f}\right)}\int_{\frac{1}{2f}^+ + \frac{n}{f}}^{0^- + \frac{n+1}{f}} I_Z(t)dt = \frac{1}{\left(\frac{1}{f}\right)}\int_{0^+ + \frac{n}{f}}^{\frac{1}{2f}^- + \frac{n}{f}} I_2(t)dt = \frac{I_L}{2} \tag{B.11}$$

P_{IN} for a single-stage circuit can now be expressed in terms of known quantities by substituting in Equations B.3, B.7, and B.11 into Equation B.1, giving,

$$P_{IN} = 2\left(C_{PAR,BP} + \frac{C_{PAR,TP}C_{PUMP}}{C_{PUMP} + C_{PAR,TP}}\right)VDD^2 f + I_L\left(\frac{C_{PUMP}}{C_{PUMP} + C_{PAR,TP}}\right)VDD + I_L V_{IN} \tag{B.12}$$

An expression for V_{OUT} is given by Equation B.13, which is obtained by reorganizing Equation B.4 and substituting in Equation B.6 for ΔV_Y and Equation B.2 for ΔV_{TP}.

$$V_{OUT} = V_{IN} + \left(\frac{C_{PUMP}}{C_{PUMP} + C_{PAR,TP}}\right)VDD - I_L\frac{1}{2f(C_{PUMP} + C_{PAR,TP})} \tag{B.13}$$

Now consider a DVS/voltage-doubler circuit with N-stages. In order to extrapolate Equations B.12 and B.13 to multi-stage operation, it must be assumed that during steady-state operation the voltages observed at all intermediate nodes don't change (like V_{OUT} is assumed to behave in the single-stage model). This is a reasonable assumption, considering the purely differential operation of adjacent DVS/voltage-doubler stages along a given charge-sharing path; i.e. when the top-plate voltage of a given C_{PUMP} is boosted up, the top-plate voltage of the C_{PUMP}

of the next stage (which it will charge share with) is reduced by the same magnitude, maintaining a virtual short between the two capacitors/stages if all switch resistances are equal. Accordingly, the parasitic capacitance at these intermediate nodes can be ignored. With said assumption disclosed, Equations B.14 and B.15 approximate P_{IN} and V_{OUT}, respectively, for an N-stage circuit, and these expressions can be used to estimate power-conversion efficiency (Equation B.16).

$$P_{IN} = 2N \left(C_{PAR,BP} + \frac{C_{PAR,TP}C_{PUMP}}{C_{PUMP} + C_{PAR,TP}} \right) VDD^2 f + NI_L \left(\frac{C_{PUMP}}{C_{PUMP} + C_{PAR,TP}} \right) VDD + NI_L V_{IN} \quad \text{(B.14)}$$

$$V_{OUT} = V_{IN} + N \left(\frac{C_{PUMP}}{C_{PUMP} + C_{PAR,TP}} \right) VDD - I_L \frac{N}{2f(C_{PUMP} + C_{PAR,TP})} \quad \text{(B.15)}$$

$$\varepsilon = \frac{I_L V_{OUT}}{P_{IN}} = \frac{I_L V_{IN} + N\left[\left(\frac{C_{PUMP}}{C_{PUMP} + C_{PAR,TP}} \right) I_L VDD - \frac{I_L^2}{2f(C_{PUMP} + C_{PAR,TP})} \right]}{N\left[2\left(C_{PAR,BP} + \frac{C_{PAR,TP}C_{PUMP}}{C_{PUMP} + C_{PAR,TP}} \right) VDD^2 f + I_L \left(\frac{C_{PUMP}}{C_{PUMP} + C_{PAR,TP}} \right) VDD + I_L V_{IN} \right]} \quad \text{(B.16)}$$

For the DVS circuit used in the proposed neural stimulator, $V_{IN} = 0$. This simplifies Equations B.14, B.15, and B.16 to Equations B.17, B.18, and B.19, respectively.

$$P_{IN} = 2N \left(C_{PAR,BP} + \frac{C_{PAR,TP}C_{PUMP}}{C_{PUMP} + C_{PAR,TP}} \right) VDD^2 f + NI_L \left(\frac{C_{PUMP}}{C_{PUMP} + C_{PAR,TP}} \right) VDD \quad \text{(B.17)}$$

$$V_{OUT} = N \left(\frac{C_{PUMP}}{C_{PUMP} + C_{PAR,TP}} \right) VDD - I_L \frac{N}{2f(C_{PUMP} + C_{PAR,TP})} \quad \text{(B.18)}$$

$$\varepsilon = \frac{\left(\frac{C_{PUMP}}{C_{PUMP} + C_{PAR,TP}} \right) I_L VDD - \frac{I_L^2}{2f(C_{PUMP} + C_{PAR,TP})}}{2\left(C_{PAR,BP} + \frac{C_{PAR,TP}C_{PUMP}}{C_{PUMP} + C_{PAR,TP}} \right) VDD^2 f + I_L \left(\frac{C_{PUMP}}{C_{PUMP} + C_{PAR,TP}} \right) VDD} \quad \text{(B.19)}$$

APPENDIX C: R-C MODEL OF DVS CIRCUIT

The Appendix B steady-state operational model for a dynamic voltage supply (DVS) circuit in the SOURCE setting, or another voltage-doubler circuit employing complementary switching pathways, assumes complete charge-transfer every switching cycle and does not take into account the ON-resistance of the top-plate switches and bottom-plate driving buffers. Accordingly, unless the devices used to implement the circuit are oversized (which would reduce power-conversion efficiency), the Appendix B model cannot be used to precisely predict the output voltage of an N-stage DVS; error should also be expected in predicting the DVS input power, although such error could be made small if scaling functions are used which relate the size of the lumped top-plate and bottom-plate parasitics of a single-stage circuit ($C_{PAR,TP}$ and $C_{PAR,BP}$, respectively) to the size of C_{PUMP} and the maximum frequency of the input pulse signals, Φ_A and Φ_B. So although the Appendix B model is useful for narrowing the DVS design space when searching for an "optimal" design, it fails to give the designer insight into the effects that different top-plate switch and bottom-plate buffer device-sizing may have on the efficiency and output voltage performance of the resulting DVS circuit; insight that may be critical in terms of choosing the C_{PUMP} size, maximum Φ_A, Φ_B frequency, and number of DVS stages (N). Accordingly, in this appendix an R-C model of the DVS (in the SOURCE setting) is presented which can be used to precisely predict the power-supplying, steady-state performance of a multi-stage DVS (or similar voltage-doubler circuit).

Figure C.1 shows a simplified schematic of multi-stage DVS in the SOURCE setting (input of first stage set to V_{IN}) loaded by a constant current I_L, with the expected flow of current after a Φ_A (Φ_B) rising edge (falling edge) or Φ_B (Φ_A) rising edge (falling edge) illustrated.
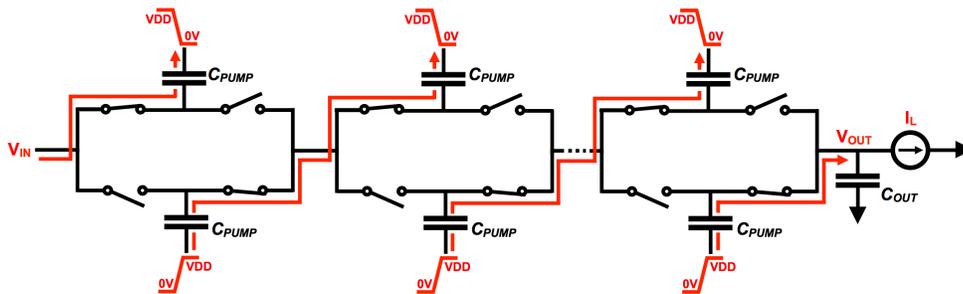

Figure C.1. Illustration of current flow in multi-stage DVS circuit in SOURCE setting (or voltage-doubler) loaded by I_L and terminated by large C_{OUT}.

Considering that said pulses are applied to the bottom-plate of a given C_{PUMP} via a CMOS inverter (i.e. the output inverter of a bottom-plate diving buffer), the conduction pathways illustrated in Figure C.1 can be represented by the schematics shown in Figure C.2, which account for switch ON-resistance and parasitic capacitances.
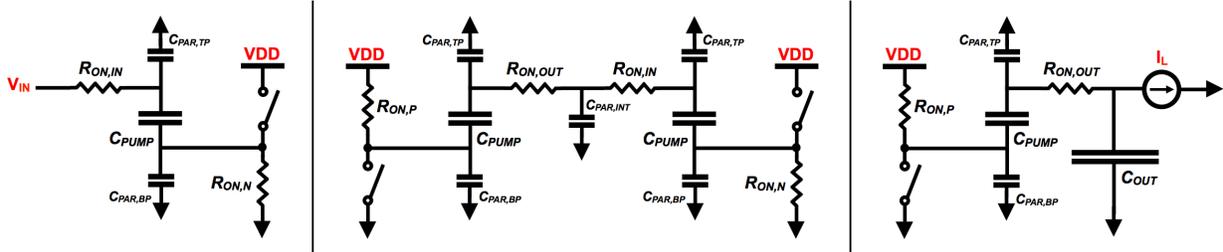

Figure C.2. Schematic representation of charge-sharing R-C networks in multi-stage DVS circuit (or voltage-doubler).

In Figure C.2, $R_{ON,IN}$ and $R_{ON,OUT}$ are the average ON-resistances of the top-plate switches within a given conduction path of a single-stage circuit. Accordingly, specific to the DVS single-stage circuit (Figure 4.3 in Chapter 4), $R_{ON,IN}$ is the average ON-resistance of the M_{N1} (M_{N2}) device and $R_{ON,OUT}$ is the average ON-resistance of the in-parallel M_{N3} and M_{P1} (M_{N4} and M_{P2}) devices (when the circuit is operating in the SOURCE-setting). $R_{ON,N}$ and $R_{ON,P}$ are the average ON-resistance of the NMOS and PMOS devices, respectively, which make up the output inverter of the buffer which drives the bottom-plate of each C_{PUMP}. $C_{PAR,TP}$ and $C_{PAR,BP}$ are the lumped top-plate and bottom-plate parasitic capacitances, respectively, within a given single-stage circuit in the SOURCE-setting, and $C_{PAR,INT}$ is the lumped parasitic capacitance which exists between adjacent stages in a multi-stage circuit.

If the transistors making up the DVS switches are sized to make $R_{ON,N} = R_{ON,P} = R_1$ and $R_{ON,IN} = R_{ON,OUT} = R_2$, then at steady-state operation (i.e. the average current supplied by each stage equals I_L), the R-C circuit appearing in the middle of Figure C-2 becomes a differential circuit, and half-circuit theory can be subsequently used to simplify it. Accordingly, this sizing condition is beneficial in that it also makes $C_{PAR,INT}$ invisible to the steady-state operation of the circuit, preventing CV^2f losses associated with this parasitic from being observed during power-supply operation.

Accordingly, if the DC offset to the first stage (V_{IN}) is ignored and C_{OUT} is assumed to be much greater than C_{PUMP}, then at steady-state, all of the charge-transfer circuits shown in Figure

C.2 can be represented by the Figure C.3 circuit (or the complementary half-circuit in which R_1 is connected to ground at t = 0 instead of VDD).
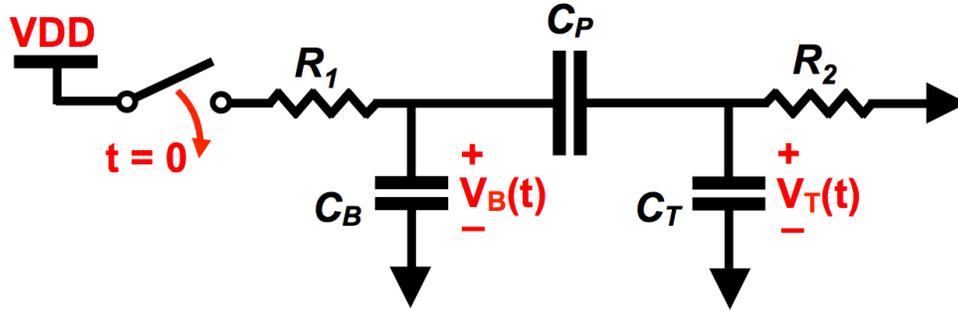

Figure C.3. Charge-transfer circuit that can be used to precisely model DVS/voltage-doubler steady-state operation.

In Figure C.3, $C_B = C_{B,PAR}$, $C_T = C_{T,PAR}$, $C_P = C_{PUMP}$ (for brevity), and t = 0 represents the time at which the bottom-plate of a C_{PUMP} capacitor is driven upwards to VDD by closing the PMOS switch of the bottom-plate driving inverter. Likewise, in the complementary half-circuit to Figure C.3, t = 0 represents the time at which the bottom-plate of C_{PUMP} is driven down to ground by closing the NMOS switch of the bottom-plate driving inverter. Considering the Figure C.3 circuit and assuming a charge-transfer interval of 1/(2f), if the conditions in Equation C.1 are used (which account for I_L loading at steady-steady operation) numerical solutions for Equations C.2 and C.3 can be found by solving the corresponding differential equations. The resulting numerical solutions for Equations C.2 and C.3 should provide precise estimates of output voltage and input power for an N-stage DVS in the SOURCE setting (or an N-stage voltage-doubler), which can then be used to calculate the expected power-conversion efficiency.

$$V_B(0) = VDD - V_B\left(\frac{1}{2f}\right), \quad \frac{1}{R_2}\int_{t=0}^{1/2f} V_T(t)dt = I_L \tag{C.1}$$

$$P_{IN} = V_{IN}I_L + 2Nf\frac{VDD}{R_1}\int_{t=0}^{1/2f}[VDD - V_B(t)]dt \tag{C.2}$$

$$V_{OUT} = V_{IN} + N\left[V_T\left(\frac{1}{2f}\right) - V_T(0)\right] \tag{C.3}$$