A Scalable, Highly-Multiplexed Delta-Encoded Digital Feedback ECoG Recording Amplifier with Common and Differential-Mode Artifact Suppression

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Abstract

We present a scalable, highly multiplexed CMOS electrocorticography (ECoG) recording front-end capable of differential-mode and common-mode artifact suppression. The front-end digitally delta-encodes 8-bit data converters to achieve 14-bit resolution. A single, shared mixed-signal front-end is time-division multiplexed to 64 differential input channels; this reduces channel area by 10x compared to the state-of-the-art. A return-to-zero scheme effectively eliminates channel crosstalk. We present performance and in-vivo measurement results of a 65nm CMOS test-chip implementation of the proposed architecture.

Keywords: time-division multiplexing, delta-encoding, ECoG

Introduction

Chronic brain computer interface (BCI) applications face several key engineering challenges. Future BCIs will require both high electrode density and large spatial coverage, resulting in thousands of electrodes [1]. BCIs require closed-loop neuromodulation, which generates large stimulation artifacts that obfuscate important signals shortly after stimulation. Power density requirements due to tissue heating remain restrictive, particularly in monolithic solutions. Additionally, a single-chip solution with efficient operation for both electrocorticography (ECoG) (<500Hz signals) and single neuron recording (<10kHz signals) is highly desirable.

We demonstrate a channel, process and frequency scalable, recording system in standard TSMC 65nm CMOS. Key contributions of this architecture to the state-of-the-art are: 10x higher recording channel density by using highly multiplexed recording channels; robust operation that combines low-precision data conversion to achieve high-precision recording; real-time common-mode and differential-mode artifact suppression at the amplifier inputs. The system scales gracefully in frequency and channel-count without significantly affecting efficiency, making it useful for a variety of biopotential acquisition applications.

Multiplexed Digital-Feedback Amplifier

Fig. 1 shows an overview of the recording architecture, which exploits the unique $1/f^n$ ($2<n<4$) power spectral density (PSD) characteristics of ECoG data in a digital-feedback architecture. In contrast with existing digital feedback schemes that require high precision oversampling converters [2], the proposed architecture uses delta-encoding to track *differences* between successive samples. This significantly reduces the ADC dynamic range requirement for a signal dominated by large low-frequency signal content. Voltage-subtraction is enabled through digital storage for each channel with an 8-bit feedback DAC. Delta-encoding allows an 8-bit Nyquist-rate ADC to provide the 80dB dynamic range required for ECoG signal acquisition. The signal can be reproduced by adding the stored signal state to the ADC output (the digitized delta-encoder residue). A one-time calibration is sufficient to handle systematic DAC nonlinearity.

This digital feedback architecture makes it possible to multiplex many feedback networks using compact memory storage. A detailed architectural description is shown in Fig. 2. Charge sampling in the amplifier eliminates the added power requirements of 7τ settling due to context switching between channels. Sample precision is determined by clock jitter, which is easily controlled at target sampling rates. A return-to-zero scheme at the inputs is implemented to eliminate crosstalk between channels (<-75dB) and provide a uniform DC coupled switched-capacitor input resistance. Use of a single amplifier for recording an array of channels allows for correlated double-sampling using a dummy channel to reduce flicker noise if required by the application.

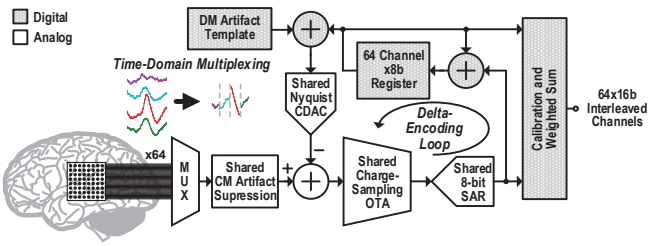

Fig. 1 Functional block diagram of the highly-multiplexed, digitally-delta-encoded ECoG signal chain with common mode and differential mode artifact suppression.

The current-reuse amplifier topology leverages the high voltage supply needs of a stimulator on a monolithically integrated chip to operate at 2.5V. This allows a large amplifier device stack using thick-oxide devices, which improves noise efficiency and CMRR without gate-leakage concerns. The amplifier output is AC coupled to a SAR ADC operating at 0.5V. The sampling-frequency-dependent input resistance (10-100MΩ) forms a high-pass corner with the series electrode capacitance (C_E) that is <1Hz for most electrodes and sampling rates. In rare situations where the high-pass corner is >1Hz, digital filtering can be effectively used to equalize the signal, exploiting the high SNR at low frequencies.

Artifact Cancellation

The feedback DAC is also leveraged to enable differential stimulation artifact suppression at the amplifier inputs. A template subtraction method is implemented to demonstrate how this architecture enables differential artifact suppression techniques that do not require a large amplifier dynamic range.

Large common-mode (CM) artifacts on the order of 100mV are often overlooked but can also degrade performance, particularly with the noise-efficient open-loop amplifiers employed in neural recording. We propose a passive, switched-capacitor technique (Fig. 2) for CM artifact suppression (CMS) to stabilize the amplifier operating point and preserve differential gain. During pre-sampling, the CM signal is extracted by a switched-capacitor network and subtracted from the input signal, canceling it before amplification. During CMS, the technique temporarily adds kT/C noise to the recording, degrading resolution by ~2 bits and reducing input impedance by ~10x. These are acceptable tradeoffs for known use-cases that require CMS.

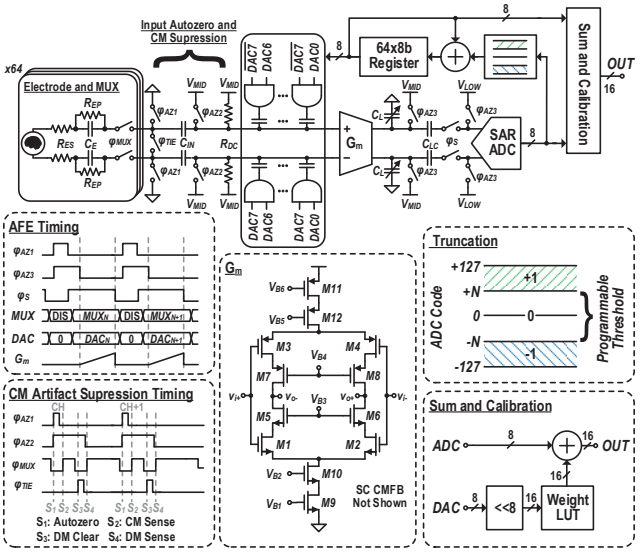

Fig. 2 Implementation and operational details of the delta-encoded multiplexed front end.

Results

The system was fabricated in a 65nm CMOS process. For bench measurements, a PtIr µWire is emulated with R_{ES} = 7.5kΩ, C_E = 820pF, and R_{EP} = 5GΩ. Fig. 3 shows a measured signal recording of a nearly full-scale 35mV$_{rms}$ sinusoid applied at the inputs. Fig. 4 shows the PSD output of a pair of sinusoidal tones demonstrating operation through multiple DAC codes. Fig. 5 shows in-vivo operation of 3/64 channels simultaneously acquired via the same multiplexed front-end. Fig. 6 demonstrates the CM and DM artifact suppression capabilities of the chip. Comparisons of this prototype to recent related works are presented in Table I. A die photo of the prototype is shown in Fig. 7.

We have demonstrated a delta-encoded digital feedback ECoG amplifier with both CM and DM artifact suppression capabilities. The delta-encoding architecture enables a large dynamic range using low-resolution data converters and enables high-density multiplexing to reduce area. Additional measurements demonstrate frequency scalability from 1kHz to 30kHz to allow flexible usage for different biopotential applications. The resulting prototype performance is comparable to the state of the art with a 10x reduction in area per channel.

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References

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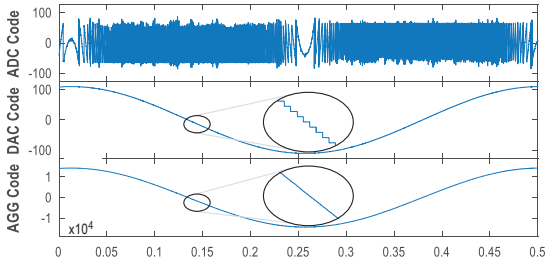

Fig. 3 Demonstration of the ADC+DAC aggregation for a 2Hz, 35mV$_{rms}$ sinusoidal input. The ADC residue interpolates the coarsely quantized DAC signal to create a 14-bit aggregated output.

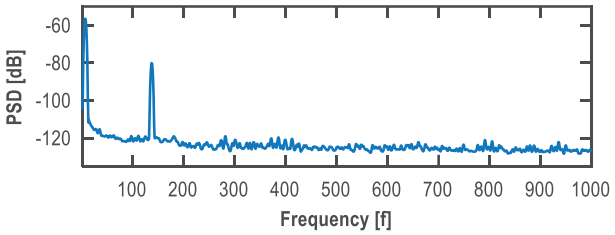

Fig. 4 PSD of a two-tone input at 7Hz, 3mV$_{rms}$ and 137Hz, 200µV$_{rms}$ showing performance across ±10 DAC codes. Minor harmonic disturbances are seen above the noise floor due to the periodic nature of DAC transitions for nonrandom signals.

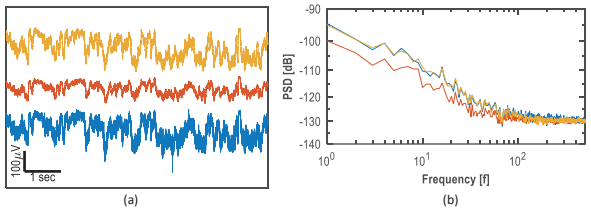

Fig. 5 Simultaneously acquired multiplexed in-vivo measurements from the motor cortex of a sedated macaque monkey on a single front end. Results in time (a) and frequency (b) domain on 3/64 channels.

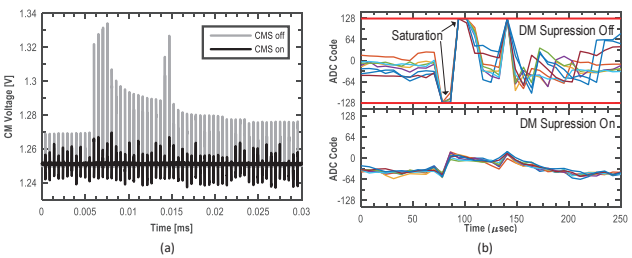

Fig. 6 (a) demonstrates in-vivo common mode artifact suppression at the amplifier inputs for 3/64 active channels. (b) demonstrates in-vivo differential mode suppression of stimulation artifacts into the linear range of the ADC. Samples acquired from a sedated macaque.

TABLE 1: COMPARISON TO STATE-OF-THE-ART

Work	UC Berkeley JSSC '15 [2]	Univ. of Michigan JSSC '16 [3]	National Chiao Tung Univ. JSSC '14 [4]	IMEC ESSCIRC '16 [5]	**THIS WORK**
Technology	65nm CMOS	0.18µm CMOS	0.18µm CMOS	0.13µm CMOS	65nm CMOS
Supply Voltage	0.5V	0.5V, 1V	1.8V	1.2V, 1.8V	0.5V, 2.5V
DM Artifact Suppression	None	LMS on Input DAC	None	None	Template Subtraction on Input DAC
CM Artifact Suppression	None	None	None	None	**Switched-Cap. Offset Correction**
Multiplexing	N/A	N/A	ADC	Shank Interconnect	**Full Signal Chain**
# of Ch.	64	8	8	768	64
Ch. Area	0.025mm^2	0.17mm^2	N/A	0.12mm^2♦	**0.0023mm^2**
Ch. Power	2.3µW	330nW	56.7µW	3µW	2.98µW
IRN/NEF	1.2µV$_{rms}$ / 4.76	3.05µV$_{rms}$ / 1.63	5.2µV$_{rms}$■/ 1.77■	12.4µV$_{rms}$■/ 8.5■	2.78µV$_{rms}$/ 2.35
CMRR/PSRR	88dB / 67dB	N/A	N/A	N/A	76dB / 82dB
Bandwidth	1Hz - 500Hz	1Hz - 2kHz	0.1Hz - 0.7kHz	0.5Hz – 8kHz	1Hz▲ – 1kHz
Pk-Pk Range	100mV$_{pk-pk}$	N/A	N/A	N/A	110mV$_{pk-pk}$
Crosstalk	-85 dB	N/A	N/A	-63dB	< -75dB
ADC Type	15b RO-Based	10b Range Adapting SAR	10b Delta-Modulated SAR	10b SAR	**8b SAR + Delta Encoding (14b)**

■*Amplifier Only* ♦*Full Probe* ▲*DC coupled to Electrode*

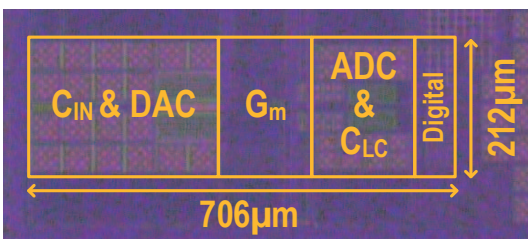

Fig. 7 Chip photomicrograph.